# RE 662 ISDN Layer II Encoder and RE 663 ISDN Layer II Decoder Service Manual

# *RE 662 ISDN Layer II Encoder and RE 663 ISDN Layer II Decoder Service Manual*

## SAFETY PRECAUTIONS FOR LINE-POWERED EQUIPMENT

All electrically powered equipment can be dangerous. At RE TECHNOLOGY AS we have taken great care to ensure safety during the design and production of our equipment. Incorrect installation, handling, or interference, can, however, be hazardous.

## INSTALLATION

This is a Safety Class I product which requires protective earthing. Normally this is obtained by the use of an IEC 320 power inlet together with a 3-wire power cable, but if the building's power installation does not include a protective earth, a separate earth connection must be established. The protective action must not be impaired by use of an extension cord (power cable) without a protective conductor. Even if the unit requires separate signal grounding, through external connections to the unit chassis, the protective earth may not be disconnected. Ensure that the line fuses have the correct value according to the voltage and power consumption.

## WARNING

Disconnecting the protective earth conductor, inside or outside the equipment, is potentially hazardous to the operator. Removing the covers may expose parts carrying dangerous voltages.

## SERVICE

Only trained service personnel should attempt to dismantle and repair the unit. Take great care during the installation and service of the unit, especially when adjusting or measuring an open unit under voltage. Before removing any covers, switch off the unit and remove the line cable from the power outlet.Capacitors inside the unit may hold dangerous charges for a considerable time after the unit has been switched off. If it is necessary to replace components in the line connected partition or area, use only new parts of the correct and approved type. Take special care to maintain or re establish the protective earthing.The conductivity must be measured after the service or repair is finished. Do not remove any warning labels, but replace any damaged or illegible warning labels with new ones.

## ESD (Electrostatic Discharge)

RE TECHNOLOGY products contain electrostatic sensitive components. You should not attempt to open a unit without proper precautions against electrostatic discharge, that is use a wrist strap and conductive work-bench surface. Otherwise the unit may fail or be degraded!

## BACK-UP BATTERIES

The estimated lifetime of the battery is four years. For units with lithium back-up batteries ensure, when replacing them, that they are of the same type and are correctly installed before you switch the power on to the unit. Do not recharge the batteries or expose them to temperatures above 100 *C (212 *F). Dispose of used batteries according to your national/local regulations. The batteries contain chemicals which can be harmful to the environment. When you dispose of the unit itself, first remove the batteries and dispose of them separately.

## EMC REQUIREMENTS

To meet the EMC requirements of Directives 89/336/EEC and 92/31/EEC you must use correctly shielded cables of good quality for all external connections when installing the unit. This implies that all multi-connector cables must have conductive connector housings with shield clamps, and the coaxial cables must be of the double-braided type.

## SAFETY SYMBOLS

Warning. The unit will be marked with this symbol when it is necessary for the user to refer to the manual.

Ground terminal (sometimes used in the manual to indicate circuit common connected to the chassis).

Attention. Observe precautions for handling Electrostatic Sensitive Devices.

Danger. Live voltage exceeding 1000 V.

Warning label for laser radiation. The product is marked with this symbol if it is necessary to protect against laser radiation which is invisible and can cause permanent damage to the eye.

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# 1. Introduction

The purpose of this Service Manual for the RE 662 and RE 663 ISDN Layer II Codec is to provide all information necessary to:

- Understand the principles of operation for the RE 662 and RE 663.
- Carry out preventive maintenance, regular adjustments and calibration.

The Service Manual provides detailed descriptions of the electrical and mechanical features of the RE 662 and RE 663.

All operating instructions as well as installation instructions are described in the "RE 662 ISDN Layer II Encoder and RE 662 ISDN Layer II Decoder", Operator Manual.

## 1.1 General Description

The RE 662 and RE 663 Codec is a full-featured audio codec that is intended for cost-effective transportation of audio signals on ISDN networks. Each ISDN Basic Rate Interface offers the user access to two unrestricted bi-directional 64 kbit/s channels at a cost comparable to that of standard telephone lines.

The RE 662 Encoder and RE 663 Decoder can encode and decode a stereo or two-channel mono program according to the ISO/IEC 11172-3 Layer II standard. It can also encode and decode a mono signal according to the ITU-T Rec. G.722 standard. The codec accepts standard analog audio formats, and if you have the digital audio option installed, it also accepts digital AES/EBU or S/PDIF audio formats.

The Layer II bit reduction technique enables transmission of a medium-quality audio signal using as little as 64 kbit/s, and hence stereo or dual-channel transmission using both 64 kbit/s circuits (B-channels) in a single basic rate.

For applications where a higher sound quality is required, the 384 kbit/s option can be installed. The codec is then capable of combining up to three Basic Rate Interfaces into a virtual higher bit-rate, a feature which allows the codec to operate at bit rates up to 384 kbit/s.

For inter-networking with 56 kbit/s networks (for example the North American Switched-56) a V.110 rate adaption protocol is used to rate-adapt up to two B-channels to 56 kbit/s transmission yielding a virtual bit rate of 112 kbit/s.

As ISDN is a bi-directional network, the encoder can be combined with an RE 661 Layer II Decoder to use bi-directional operation. Similarly, the decoder can be combined with the RE 660 Layer II Encoder. Alternatively, the reverse direction (from decoder to

encoder) can be accessed via two 64 kbit/s RS-422 interfaces. Note, that this requires a particular factory configuration and must be specified when placing the order for the codec.

In any aspect of audio transmission, the RE 662 and RE 663 Codec offers high quality and reliability. Contribution of programs, such as TV news feeds, weather reports, remote pick-ups, satellite back hauls, coverage of concerts, festivals or stadium events, is one main application.

Another main application of the codec is program distribution, such as studio-to-studio connections, Studio-to-Transmitter Links (STL), Inter City Relays (ICR) and satellite and microwave transmissions.

To serve the need for additional data capacity, the codec provides an in-band asynchronous RS-232 data channel.

# 2. Principle of Operation

## 2.1 General Description

This chapter describes the various circuits in the RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder, thus making it easier for the reader to understand the codec's overall concept.

Detailed descriptions of the individual circuits in the RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder are found in Chapters 4 to 8.

An RE 662 ISDN Layer II Encoder comprises two to four circuit boards: a Layer II encoder board, a triple basic rate interface board and, if the 384 kbit/s option is installed, a B-channel equalizer board. Furthermore, a small digital input option board can be installed.

The triple basic rate interface connects directly to ISDN and is able to connect and disconnect B-channels (64 kbit/s). The triple basic rate interface is able to handle up to 6 B-channels, yielding a total transmission capacity of 384 kbit/s.

If the 384 kbit/s option is installed, the B-channel equalizer's task is to split a serial data signal conveying the Layer II frames into a number of parallel 64 kbit/s data streams, one for each established B-channel. In addition the B-channel equalizer performs the reverse operation by combining the received B-channels to restore the original Layer II data signal after having equalized possible delay inequalities of up to 0.5 s between the established B-channels. This feature is used to feed an RE 661 Decoder with received data in order to form a bi-directional link

The Layer II Encoder board is equivalent to the one used in the RE 660 Layer II Encoder. The board accepts up to two audio input signals which are compressed according to ISO/IEC 11172-3 Layer II specification to a bit-rate matching the capacity of the established B-channels. I digital input option is mounted directly on the Layer II encoder board.

An RE 663 ISDN Layer II Decoder also comprises two to four circuit boards; a Layer II decoder board, the same Triple ISDN Basic Rate Interface and, if the 384 kbit/s option is installed, the same B-channel equalizer board as used in the RE 662 ISDN Layer II Encoder. Furthermore, a small digital output option board can be installed.

Like the Layer II Encoder board, the Layer II Decoder board is equivalent to the one used in the RE 661 Layer II Decoder. The board accepts a restored serial data-signal conveying audio data in a format according to the ISO/IEC 11172-3 Layer II standard. The decoder decodes the Layer II audio frames and restores the audio signals. A digital output option is mounted directly on the Layer II decoder board.

Figs. 2.1 and 2.2 show schematic block diagrams of the RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder. Chapters 2.2 to 2.4 of this manual show detailed block diagrams of each board, with an associated description of the operation.

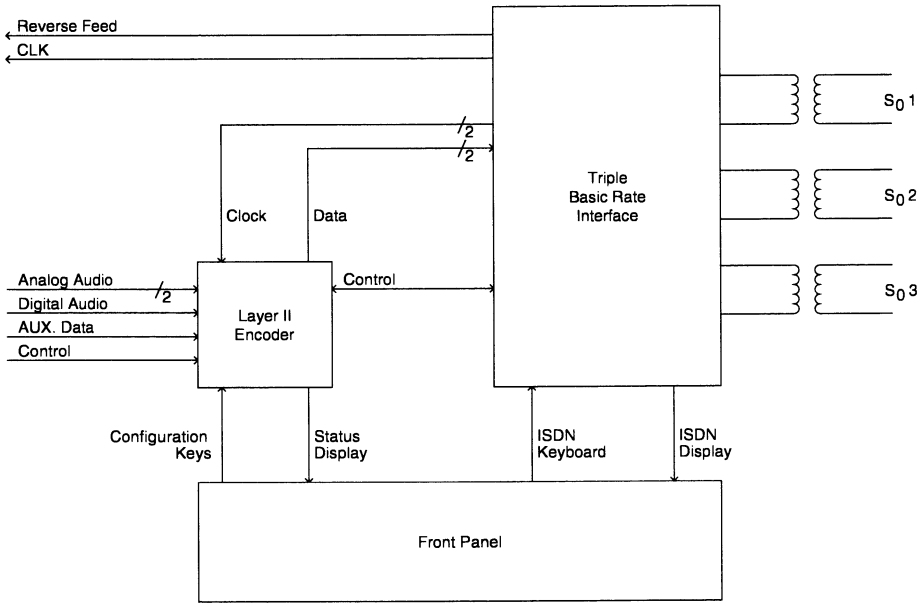


*Fig. 2.1 The RE 662 ISDN Layer II Encoder*

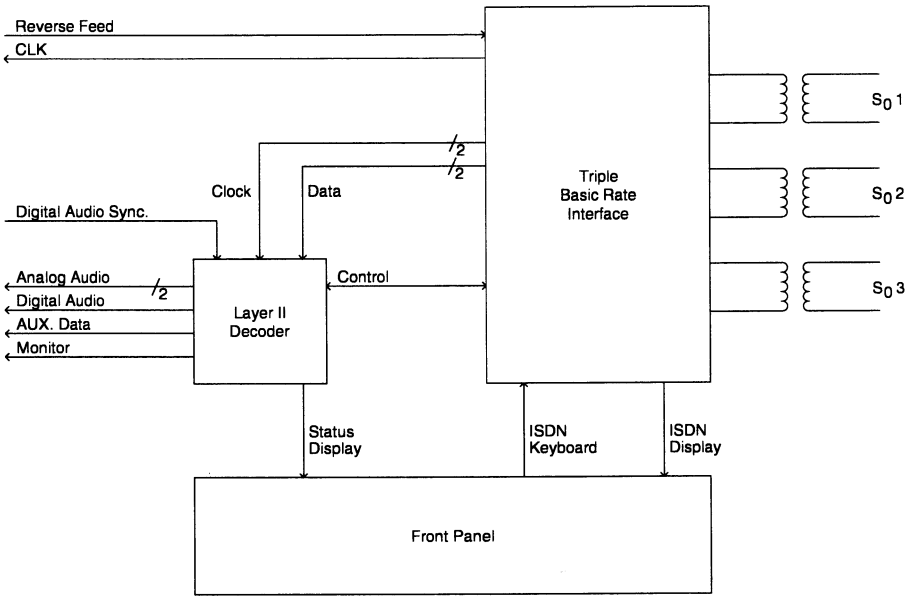


*Fig. 2.2 The RE 663 ISDN Layer II Decoder*

## 2.2 Layer II Encoder Board

Fig. 2.3 shows a schematic block diagram of the Layer II encoder board.

The Layer II encoder encodes up to two analog or a digital audio input into a serial data signal according to the ISO/MPEG Layer II specification. The rate of the Layer II encoded data signal is determined by the frequency of the input clock, from the B-channel equalizer, which will match the capacity of the established B-channels

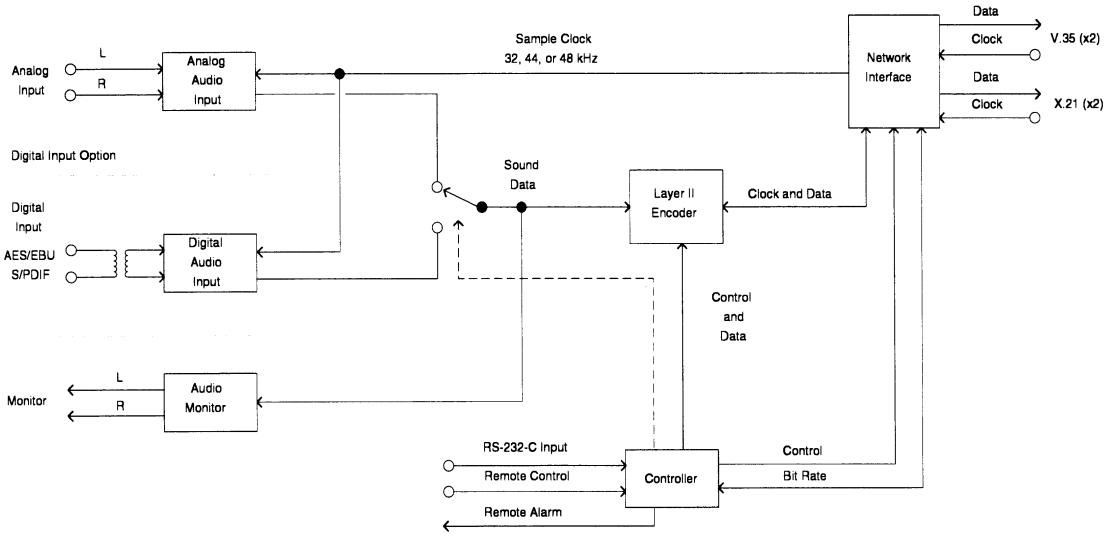


*Fig. 2.3 The Layer II Encoder Board*

### Analog Audio Input

The analog audio input circuit accepts two balanced analog audio input signals which may either be a stereo pair or up to two independent mono programs. The input signals are buffered by an amplifier with an input impedance of 600 Ω or >25 kΩ. Then the signals are low-pass filtered and amplified to accommodate a clipping level from -3 dBu to 21 dBu. The input impedance and clipping level are set by the proper configuration of a set of internally located jumpers. After amplification, the analog signals are converted into the digital domain at a rate equal to 64 times over sampling with a resolution of 16 bits per sample.

### Layer II Encoder

The controller selects either the audio data from the digital inputs sample rate converter, or from the analog inputs audio ADC to be fed to the Layer II encoder as commanded via the remote port or the front panel keys.

The audio samples enter the Layer II encoder at a rate of 32, 44.1 or 48 kHz. When 16, 22.05 or 24 kHz sampling is requested the Layer II encoder low-pass filters the input signals and decimates them by two meeting the half sample rate command.

A Layer II frame is comprised of a header field, an audio sample field and an auxiliary data field. A frame comprises 1,152 samples of audio information (per channel). The frame length (in time) only depends on the audio sample rate. The transmission bit rate determines the number of bits in each frame and hence determines the quality of the encoded audio signals.

The header field contains all the control information the decoder requires to decode the frame and to restore the original audio samples. This control information is gathered by the controller and is passed to the Layer II encoder for insertion into the frame header field.

The audio samples are filtered into 32 sub-bands and re-quantized according to a psycho acoustic measure of what can be perceived by the human ear. The result of the psycho acoustic measure is the minimum signal-to-quantization noise ratio required in each sub-band without introducing any audible impairment to the encoded signals.

An iterative process allocates bits in the frame, re-quantizes the sub-band samples to fit the allocated capacity until the minimum signal-to-quantization noise ratio is met for all sub-bands, or until the capacity of the frame is used.

When the minimum signal-to-quantization noise ratio is reached, the audio signals are transmitted, unimpaired, with a quality level equal to that which can be obtained by 16-bit linear transmission. This level of quality is, in general, reached when the transmission rate is 128 kbit/s (two B-channels) per channel or higher.

The auxiliary data channel data is located in the auxiliary data field of the frame. The selected data rate of the RS-232 channel, signaled by the controller, is formed into a code word and inserted into the frame as the first byte after the audio sample information. The Layer II encoder counts the number of auxiliary bytes to be transmitted in the frame, and inserts this number as a second code word. These two code words are followed by the auxiliary data bytes.

The formed Layer II frames are then routed to the B-channel equalizer board.

## Audio Monitor

The audio monitor receives the same audio samples as the Layer II encoder and converts them back into the analog domain.

Digital audio data placed into the encoder's digital audio input can be pre-emphasized. The digital audio data stream contains information pertaining to which specification ITU J.17 or 50/15 µs, has been used. This permits the controller to enable the appropriate de-emphasis of the audio prior to the amplification and buffering process.

The audio monitor feature permits conventional analog headphone monitoring of the digital AES/EBU or S/PDIF audio signal when the digital audio input of the encoder is being used. Additionally, when the analog audio inputs are being used, the audio monitor allows quick verification of proper operation of the audio ADC as well as a verification of whether or not the analog input's clipping level has been set appropriately.

### Clock Control

The clock control measures the frequency of the clock received from the B-channel equalizer to allow the controller to configure the control signals in the Layer II header to the appropriate transmission rate (the sum of established B-channels).

The clock control circuit generates one of three sample frequencies, 32, 44.1 and 48 kHz, locked to ISDN via the B-channel equalizer. The controller enables one of them to be used to convert the analog audio input signals into digital form, and as a reference, to synchronize the digital audio input samples to the transmission rate.

### Controller

The controller's task is to control the Layer II-related operation of the RE 662 ISDN Layer II Encoder.

Inputs supplied by the front panel keys or the remote control port, the digital audio input signal (when enabled), and the clock control circuit are used to configure and control all of the circuitry which comprises the Layer II encoder board.

## 2.2.1 Encoder Options

### Digital Audio Input

The digital audio input is a factory-installed option. It is a small, piggy-back add-on circuit board located in the upper left corner of the Layer II encoder.

The digital audio input can be set to either balanced AES/EBU or single-ended S/PDIF formats by proper configuration of a pair of internally located jumpers. A transformer provides a galvanic separation of the input from the connected digital audio source. The decoding of the digital data stream is regulated by the controller which first detects the presence of an applied signal and then measures its quality as a function of the eye height in the input signal. The validity of the audio samples conveyed in the digital audio input is checked. In the case of a faulty sample, the sample is substituted by the previous (non-faulty) sample. This minimizes the audio impairment caused by the faulty samples within the input signal.

The input digital bit stream contains control information as well as the actual audio data. This control information is decoded and forwarded to the controller so that it can be used to configure the RE 662 ISDN Layer II Encoder according to the signaled pre-emphasis of the audio, and the nature of the program. That is, a stereo program, a mono program or two independent mono programs.

Next, the audio samples are extracted and truncated to 16 bits prior to being stored in a sample rate equalizer.

The samples are then read from the sample rate equalizer at the sample frequency used to digitize the analog audio inputs.

## 2.3 Layer II Decoder Board

Fig. 2.4 shows a schematic block diagram of the Layer II decoder board.

The Layer II decoder receives the restored serial Layer II data signal from the B-channel equalizer board. The Layer II decoder board synchronizes to the data signal by means of the Layer II headers and restores the audio signals and the auxiliary data channel.

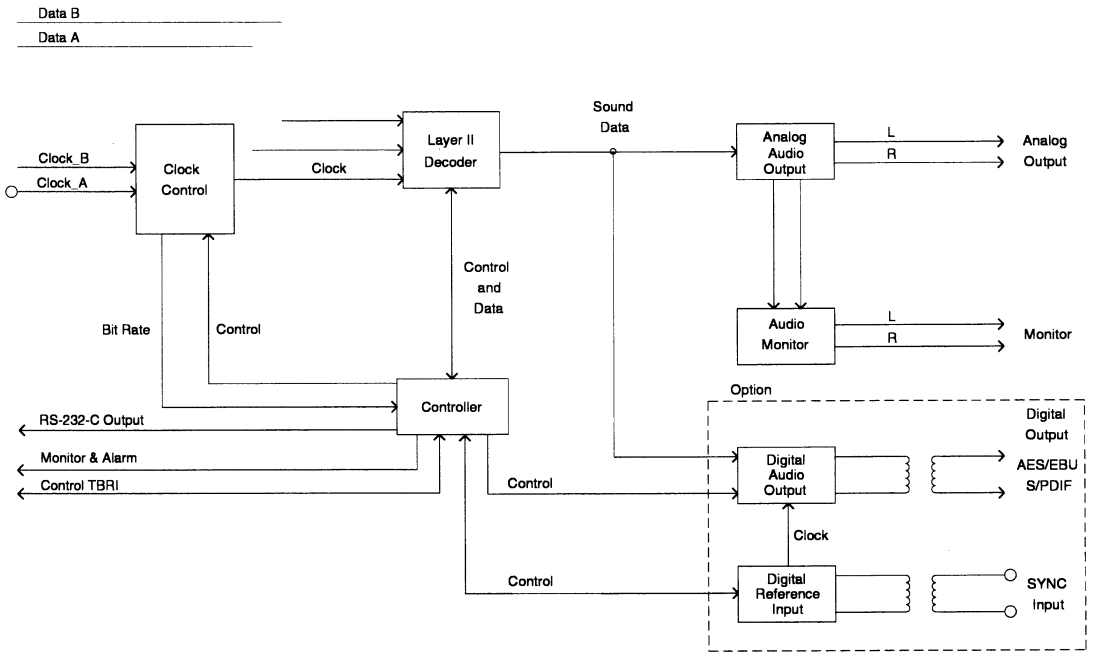


*Fig. 2.4 The Layer II Decoder Board*

## Clock Control

The clock control measures the frequency of the clock received from the B-channel equalizer or directly from the triple basic rate interface, and uses it as reference to generates the three sample frequencies, 32, 44.1 and 48 kHz. One of the three frequencies is used to convert the restored audio signals back into analog form as signaled in the Layer II header.

## Layer II Decoder

The Layer II decoder receives the serial data inputs from the B-channel equalizer or directly from the triple basic rate interface, and looks for frame alignment. When frame alignment has been achieved, the Layer II header is decoded and the control information conveyed in the frame header is routed to the controller in order for it to configure the operation of the Layer II part of the RE 663 ISDN Layer II Decoder.

The audio samples are restored using the signaled sample frequency, and are fed to the audio output circuits. If only a single mono channel is decoded, the samples are copied to utilize both the left and right analog audio outputs.

If the Layer II decoder detects one of the half sample frequencies of 16, 22.05 or 24 kHz, it interpolates the sample frequency by two before the audio samples are fed to the audio output circuits at a rate of 32, 44.1 or 48 kHz.

The data rate of the auxiliary channel is recovered from the first byte in the auxiliary data field in the Layer II frame and the second code word is used to extract the conveyed number of data bytes in each frame.

## Analog Audio Output

The analog audio output circuit receives the restored audio samples from the Layer II decoder. The audio samples are converted back into the analog domain at a rate equal to 128 times over-sampling with a resolution of 16 bits. The audio signals are lowpass-filtered to remove the high-frequency sampling mirrors, and are de-emphasized according to the ITU J.17 or 50/15 µs specification when signaled by the controller.

The signals are then amplified to give a maximum output level from -5 dBu to +21 dBu, as selected by internal jumpers, and are buffered by an amplifier with an output impedance which is jumper selectable to be either low or 600 Ω.

## Audio Monitor

The audio monitor receives a copy of the de-emphasized left and right channel audio signals from the analog audio output circuit.

The signals are volume controlled and buffered, before they are fed to the headphone jack connector on the front panel.

### Controller

The controller's task is to configure and control the operation of the Layer II decoder.

Based on control inputs from the clock control circuit and the Layer II decoder it configures the Layer II part of the RE 663 ISDN Layer II Decoder.

## 2.3.1 Decoder Options

### Digital Audio Output

The digital audio output is a factory-installed option. It is a small, piggy-back add-on circuit board located in the upper left corner of the Layer II decoder.

The digital audio output receives audio samples from the Layer II decoder in parallel with the analog audio output. The samples are stored in a sample rate converter, from where the samples are read by the Layer II conveyed sample frequency (32, 44.1 or 48 kHz), or by a sample frequency derived from the digital reference input.

The sample rate converter can convert the audio samples from one of the three standard sample frequencies to any other sample rate derived from the digital reference input.

From the sample rate converter, the samples are encoded into a digital signal according to the AES/EBU or S/PDIF specification supervised by the controller. The digital output format is selected by internal jumpers and passed to the output terminal.

### Digital Reference Input

One of the major operational difficulties when using digital audio signals is synchronization of digital audio sources. To eliminate this difficulty, the Layer II decoder accepts a reference input signal according to the AES/EBU or S/PDIF formats. This reference signal can be used to synchronize the digital audio output signal, making the digital audio output as easy to use as the analog audio outputs.

## 2.4 B-channel Equalizer Board (Option)

The 384 kbit/s option is a factory-installed option providing the codec with the B-channel equalizer board. The circuits of the B-channel equalizer board are described in Chapter 6.

Fig. 2.5 shows a schematic block diagram of the B-channel equalizer board used in both the RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder.

The B-channel equalizer is a bi-directional circuit that both splits the serial Layer II data signal into a number of parallel data signals, one for each established B-channel, and combines the received data from the B-channels to restore the serial Layer II data signal.

When included in an RE 662 ISDN Layer II Encoder, the B-channel equalizer receives Layer II data from the bottom board Layer II encoder for transmission, and outputs Layer II data received from the B-channels to the X.21 data interface for an external Layer II decoder.

Similarly, when included in an RE 663 ISDN Layer II Decoder, the B-channel equalizer feeds Layer II data to the bottom board Layer II decoder. Data to be transmitted via the ISDN B-channels is received from an external Layer II encoder connected to the X.21 data interface.

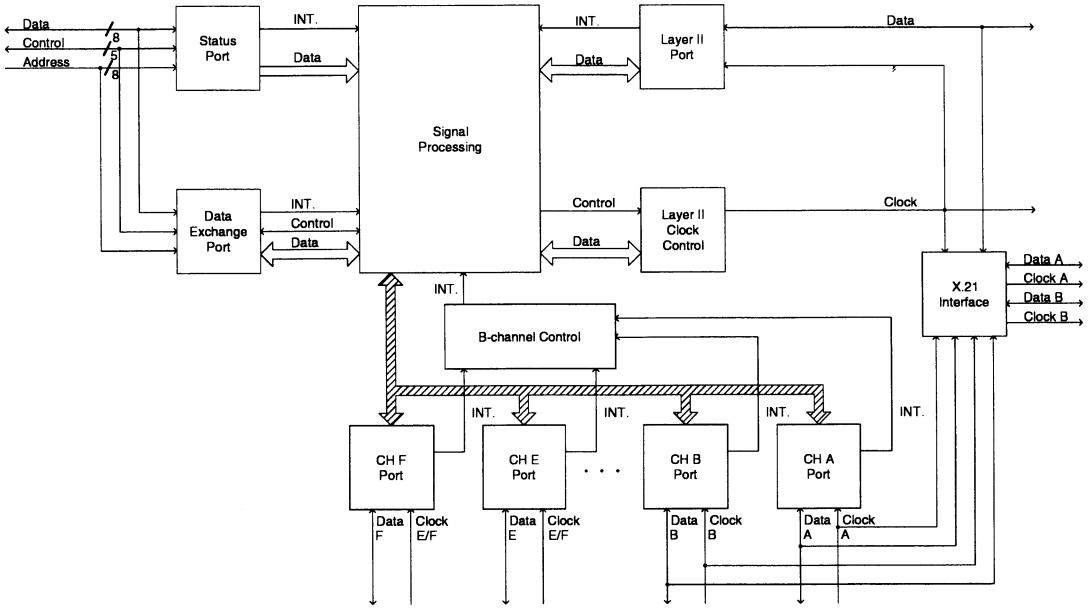


*Fig. 2.5 The B-channel Equalizer Board*

## Status Port

The triple basic rate interface controls the operation of the B-channel equalizer by writing status of the six B-channels to the status port. A status message signals which B-channels that have been established to transmit and receive data and the bit rate used on B-channels A and B (64 or 56 kbit/s). The 56 kbit/s option allows the ISDN Layer II terminal to communicate with an RE 660 Layer II Encoder or an RE 661 Layer II Decoder connected to a switched 56 kbit network.

Last, the status port holds a set of sequence numbers to be used when combining the data received from the B-channels (see below).

## Signal Processing

The B-channel equalizer is based on a DSP circuit. Upon power-up, the DSP initializes the circuitry on the board and waits for an interrupt from the status port (from the triple basic rate interface). The DSP reads the status port and configures the frequency of the Layer II clock according to the number of enabled ISDN B-channels.

The splitter function synchronizes to the input Layer II data signal and splits the Layer II frames into parallel 64 kbit/s data signals, frame by frame. The private bit located in the Layer II header is toggled to signal the receiver a multi-frame structure in each B-channel in order to permit the receiver to equalize a possible transmission delay inequality between the B-channels.

The combiner function locks to the parallel Layer II data inputs from the ISDN B-channels and decodes the private bit sequence to measure the transmission delay inequality between the individual B-channels. Next, the original Layer II data signal is restored by sequentially multiplexing the data from the B-channels frame by frame, before being routed to the Layer II decoder.

As ISDN calls are not necessarily received on the same physical B-channel as used by the caller, the ISDN Layer II terminals exchange channel identification upon establishment of a call. The channel identification codes are used to multiplex the frames from the B-channels in the same order as they were de-multiplexed before transmission. This sequence information is read by the signal processing circuit from the status port.

## Channel A, B, C, D, E, and F Ports

Each B-channel enters the B-channel equalizer 16 bits at a time by separate data ports. The data ports work as two 16 bits shift registers where data to be transmitted is written in parallel form into one shift register and shifted out as a serial data signal to the transmit direction of the B-channel. Receive data from the same B-channel is clocked into the other shift register and read by the signal processing circuit in parallel form, also 16 bits at a time.

## B-channel Controller

The B-channel controller works as an interrupt controller for the six B-channel data ports. Each B-channel port has an interrupt signaling that the port needs service (data to be read and data to be output). The six interrupts are combined into a single interrupt that interrupts the signal processing circuit. A register can be read to signal which data port that has caused the interrupt and a second register is used to clear the interrupt after service.

### Layer II Clock Control

The Layer II clock control circuit generates a clock signal to be used to collect data from the Layer II encoder board (or when installed in a decoder from an external Layer II encoder) and to feed data to an external Layer II decoder (or when installed in a decoder to the bottom Layer II decoder board).

The clock is set to either 56, 64, 112, 128, 192, 256, 320 or 384 kHz dependent on the number of enabled B-channels and the rate of B-channel A and B as signaled by the status port.

### Layer II Data Port

Layer II data from the Layer II encoder is clocked into a serial-to-parallel shift register from where the signal processing circuit can read the Layer II frames to be split before being passed to one of the B-channel data ports. As well, received and combined Layer II data from the B-channels are sent to the Layer II decoder via another shift register.

### Data Exchange Port

The data exchange port is an eight bit bi-directional port between the signal processing circuit and the triple basic rate interface. The triple basic rate interface uses the port to the signal processing circuit to write data during software updates, and the signal processing circuit uses the port to signal error messages to the triple basic rate interface in case of faults in the ISDN transmission.

### X.21 Data Interface

The X.21 interface comprises line drivers, line receivers and connectors to use the reverse feed through ISDN. Also, the circuit contains solder points which are used to configure the B-channel equalizer to operate in an RE 662 ISDN Layer II Encoder or an RE 663 ISDN Layer II Decoder, and to select reverse feed for Layer II, or for transparent 56/64 kbit/s data.

In an RE 662 ISDN Layer II Encoder, the solder points configure the X.21 connectors as outputs only, as the transmit direction carries the Layer II signal from the bottom-board Layer II encoder.

When configured for bi-directional Layer II transmission, the X.21 connector A outputs clock and the combined Layer II data at a rate equal to the transmit direction. X.21 connector B is idle in this configuration.

Alternatively, the combine function of the B-channel equalizer can be disabled, where X.21 connectors A and B are both configured to output a 56/64 kHz clock and data signals received from B-channel A and B (So1).

In an RE 663 ISDN Layer II Decoder the solder points configure the X.21 connectors into inputs only, as the receive direction carries the Layer II signal to the bottom-board Layer II decoder.

When configured for bi-directional Layer II transmission, the X.21 connector A outputs clock and inputs Layer II data from an external Layer II encoder. X.21 connector B is idle in this configuration.

Alternatively, the split function of the B-channel equalizer can be disabled, where X.21 connectors A and B are both configured to output a 56/64 kHz clock and input data to be transmitted via B-channel A and B (S01).

## 2.5 Triple Basic Rate Interface Board

Fig. 2.6 shows a schematic block diagram of the triple basic rate interface board used in both the RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder. The board interfaces directly to the ISDN S-bus and establishes ISDN B-channels to route Layer II data through the network.

The triple basic rate interface connects to the B-channel equalizer by controls and six sets of B-channel signals. A set of B-channel signals comprises a clock at 64 kHz and a transmit and receive data signal, each having a rate of 64 kbit/s.

The controls are used to signal the B-channel equalizer status on the B-channels as being ready to transmit and receive data.

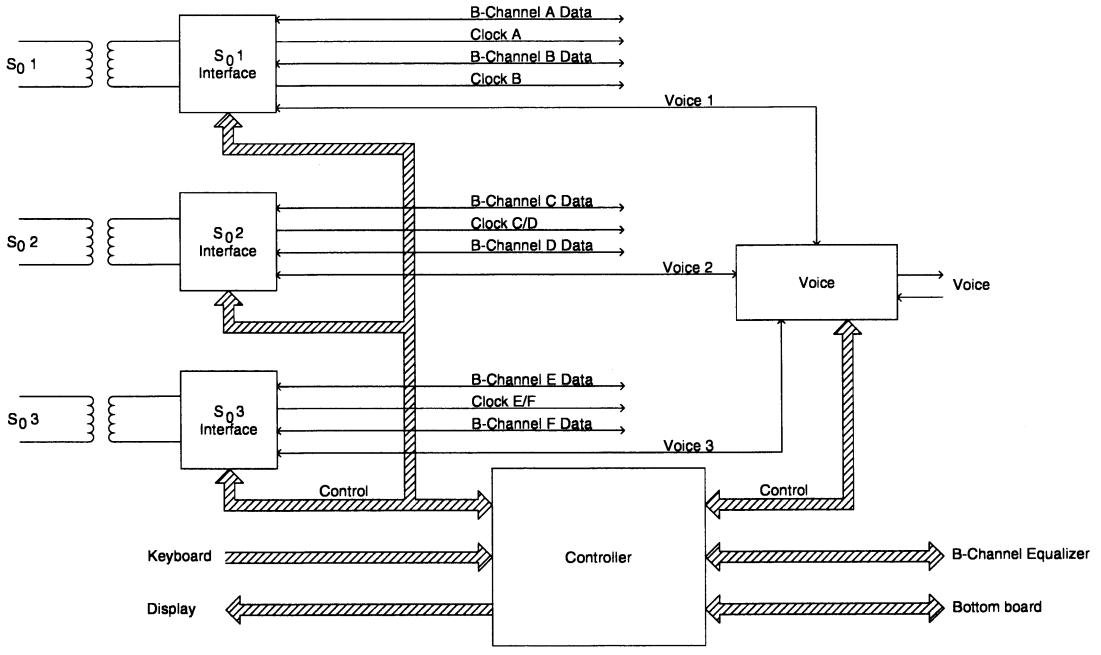


*Fig. 2.6 The Triple Basic Rate Interface Board*

## So1 ISDN Interface

The So1 interface circuit comprises a DSC (Digital Subscriber Controller) and two ITACs (ISDN Terminal Adapter Circuit), one for each of the two B-channels.

- The DSC handles the functions listed below:
- The basic rate interface to ISDN.
- Multiplexing of the two B-channels and the D-channel.
- D-channel HDLC (High Data Link Channnel) processing.
- The audio interface for the Voice channel.

The ISDN basic rate interface is a four-wire interface with separate protection circuits for the transmit and receive directions. Transformers ensure a galvanic separation between the triple basic rate interface board and the ISDN network termination (NT).

The two B-channels are time-division multiplexed with the D-channel and convey Layer II frames entered via the serial interface or voice data (ITU Rec. G.711) originating from the front panel handset.

The D-channel is used to establish and disconnect both voice and data calls as defined by the appropriate ITU recommendations.

The ITAC's are able to perform a V.110 rate conversion between the 64 kbit/s ISDN and 56 kbit/s user data. This feature allows inter-networking with RE 660 and RE 661 Layer II Codecs connected to the North American Switched 56 kbit network.

## So2 and So3 ISDN Interface

The So2 and So3 interfaces are equal to So1 with the exception of the ITACs as only So1 is able to inter-network with a 56 kbit/s network. Instead, So2 and So3 have discrete circuits to form and restore the 64 kbit/s data and clock signals to the B-channel equalizer board.

## Voice

The voice circuit comprises a buzzer and a front panel LED to signal when a call is pending. By connecting a handset to the front panel jack access is given to a 3.5 kHz telephone circuit. The controller directs the voice signals to one of the DSCs, depending on non-occupied B-channels.

## Controller

The controller controls all the circuitry of the triple basic rate interface board and configures the operation of the board according to user inputs via the front panel keyboard. The controller is based on a NEC V53 µP with flash prom program memory, static RAM data memory, and an E²PROM to hold stored telephone numbers.

When a data (Layer II) call is to be established, the controller sets up the call via one of the DSCs and configure the ITACs for the appropriate bit rate. When the ISDN exchange reports back that the circuit is established the controller transmits a "Channel Id" code to the remote unit and receive a similar code. The Channel Id code is used as sequence numbers by the combine function of the B-channel equalizer. Having exchanged Channel Id the controller sends a status message to the B-channel equalizer board to signal that a specific B-channel is established and ready for data transfer.

# 3. Dismantling

This chapter describes how to get access to the various circuits of the RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder. The encoder and the decoder are dismantled in the same way.

Reassembly is not described, as it is, in principle, just the opposite of the dismantling operation. Note however, that the tabs on the top plate must be inserted under the rim of the front panel.

To dismantle the RE 662 and RE 663 you need a pozidrive screwdriver and (for the Layer II Encoder/Decoder board) an adjustable spanner.

Fig. 3.1 shows a plan of the B-channel Equalizer and ISDN boards. The letters in parentheses after the instructions below refer to the numbers in the figure.

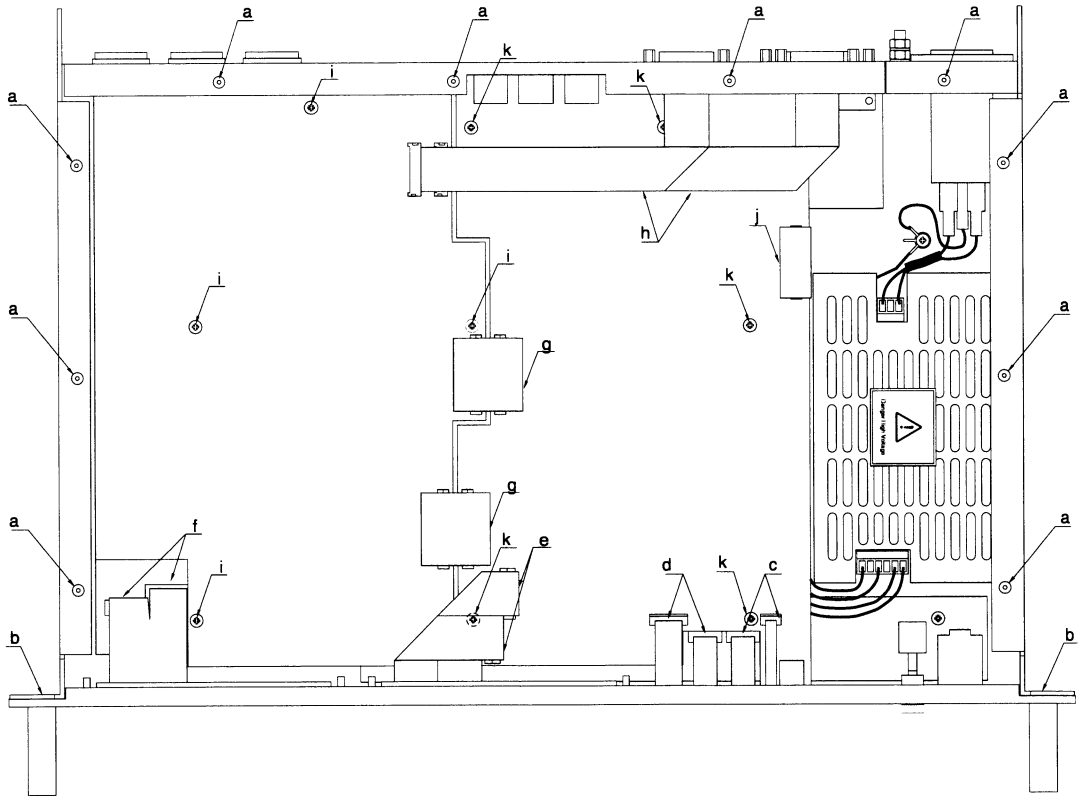


*Fig. 3.1 Plan of the B-channel Equalizer and ISDN Boards*

## 3.1 Top Plate

To remove the top plate, unscrew the ten screws marked "**a**" in Fig. 3.1. Seen from above, from left to right, are the B-channel equalizer board, the triple basic rate interface (ISDN) board and the power supply.

## 3.2 Front Panel

To remove the front panel, do as follows:

1. Remove the top plate. See Chapter 3.1 for details.
2. Unscrew the four screws which hold the front panel in position against the box. These are marked "**b**" in Fig. 3.1.
3. Disconnect the two ribbon cables which connect the ISDN board and the encoder/decoder board to the front panel LEDs. These are marked "**c**".

   To do this, first grip the two shorter edges of each PCB connector between thumb and forefinger and pull upwards. With the outer casing pulled out, pull gently on the cable to remove it. While the outer casing is pulled out, there is no resistance.
4. Disconnect the two ribbon cables which connect the ISDN board and encoder board to the front panel keyboard. These are marked "**d**".
   How to disconnect is described in step 3.

   **Note**: No cable connects the decoder board to the front panel keyboard, that is, there is only one ribbon cable.
5. Disconnect the two ribbon cables which connect the ISDN board to the ISDN display on the front panel. These are marked "**e**".

   To do this, press down on top of each connector's "spine" and, with the spine held down, pull gently on the cable to remove it. While the spine is held down, there is no resistance.
6. Disconnect the two ribbon cables which connect the encoder/decoder board to the Status display on the front panel. These are marked "**f**".
   How to disconnect is described in step 5.
   You can now remove the front panel.

## 3.3 B-channel Equalizer Board

To remove the B-channel equalizer board:

1. Remove the top plate. See Chapter 3.1 for details.
2. Disconnect the two ribbon cables which connect the B-channel equalizer board to the ISDN board. These are marked "**g**".

To do this, grip the two shorter edges of each connector between thumb and forefinger and pull upwards.

3. Disconnect the two ribbon cables which connect the B-channel equalizer board to the RE 660/661 /X21 Connector A and B ports. These are marked "**h**".
   To do this, pull the white connectors out of the board.
4. Unscrew the four screws marked "**i**".
   You can now remove the B-channel equalizer board.

## 3.4 ISDN Board

To remove the ISDN board:

1. Remove the top plate. See Chapter 3.1 for details.
2. Disconnect cables marked "**c**", "**d**" and "**e**".
   See steps 3, 4, and 5 in Chapter 3.2 for details.
3. Disconnect cables marked "**g**".
   See step 2 in Chapter 3.3 for details.
4. Disconnect the cable marked "**j**".
   To do this, grip the two shorter edges of each connector between thumb and forefinger and pull upwards.
5. Unscrew the five screws marked "**k**".
   You can now remove the ISDN board.

## 3.5 Layer II Encoder/Decoder Board

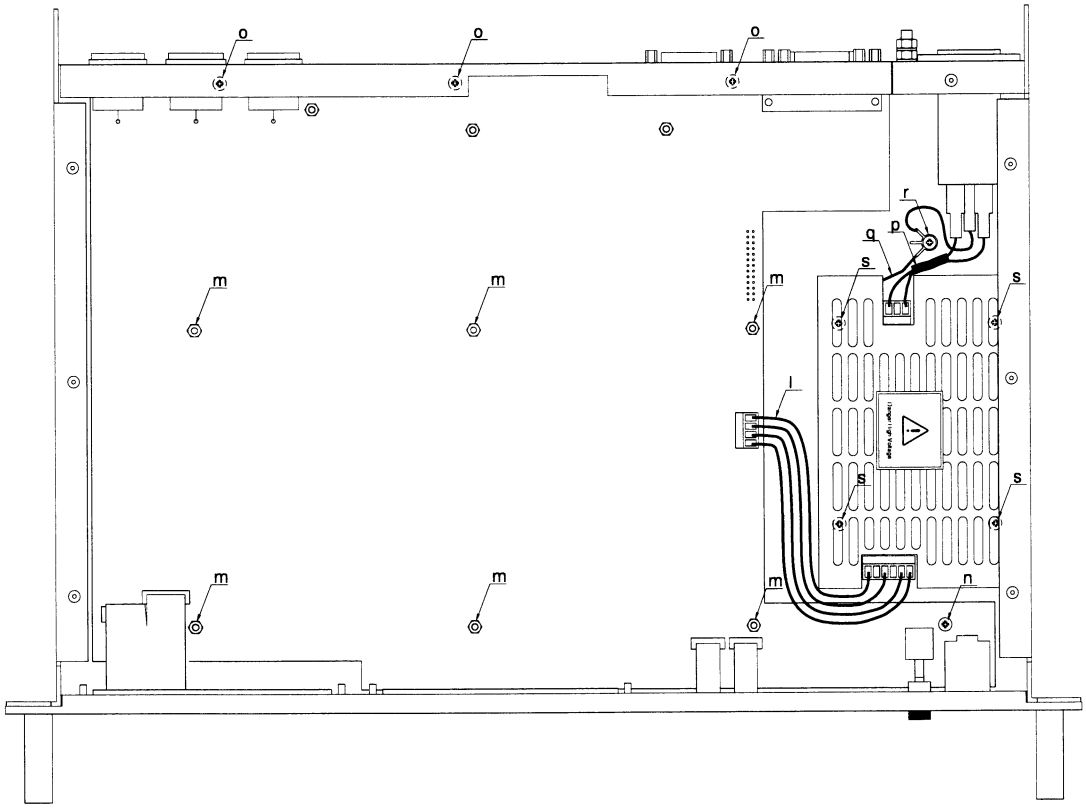


*Fig. 3.2 Plan of the Layer II Encoder/Decoder Board*

To remove the Layer II encoder/decoder board:

1. Remove the B-channel equalizer and ISDN boards. See Chapter 3.3 and Chapter 3.4 for details.
2. Disconnect the wires to the power supply. These are marked "**l**" in the figure above. To do this, press down on the side of the connector and pull the terminal out.
3. Remove the six stay bolts marked "**m**".
   To do this, use an adjustable spanner.
4. Unscrew the screw marked "**n**".
5. Unscrew the three screws on the bottom of the box marked "**o**".
   You can now pull out the encoder/decoder board and rear panel as one piece.

## 3.6 Power Supply

To remove the power supply, do as follows:

1. Remove the top plate. See Chapter 3.1 for details.
2. Disconnect the wires marked "**l**" in Fig. 3.2.
   To do this, press down on the side of the connector in the power supply unit and pull out the terminal.
3. Disconnect the wires marked "**p**" and "**q**".
   To do this, pull them out at the power input-port unit.
4. Unscrew the screw marked "**r**".
5. Unscrew the four screws on the on the bottom of the box marked "**s**".
   You can now remove the power supply unit from the box.

# 4. Layer II Encoder Circuits

## 4.1 Introduction

This chapter describes and shows the block diagrams for the Layer II encoder circuits.

A diagram showing the locations of the adjustable components in the encoder is located in Chapter 4.14.

## 4.2 Controller

### 4.2.1 General Description

The controller handles most front and rear panel input/outputs as well as being the link between various circuits in the encoder.

Input from the front panel keys or the rear panel remote connector are processed by the controller and used for the setup and control of various circuits such as the digital audio input circuits, the RS-232 input, the LCD display, the network interface and the digital signal processor (DSP).

### 4.2.2 Interfaces

The micro controller interfaces to the rest of the system through several on-chip I/O bits, externally mapped I/O ports and interrupt lines. Table 4.1 describes the on-chip I/O bits. Table 4.2 describes the decoded I/O selects from the controller circuit.

| Bit | Name | I/O | Description | Source/Destination |
|---|---|---|---|---|
| P1.0 | /KEYINT | INT | Interrupt from front panel keys on falling edge | From front panel circuit |
| P1.1 | JTCK | O | Clock bit for JTAG interface | To encoder DSP circuit |
| P1.2 | JTDI | O | Data bit for JTAG interface | To encoder DSP circuit |
| P1.3 | JTMS | O | Mode select for JTAG interface | To encoder DSP circuit |

*Table 4.1 On-Chip I/O Bits*

| Bit | Name | I/O | Description | Source/Destination |
|---|---|---|---|---|
| P1.4 | /AESINT | I | Interrupt from digital audio receiver on falling edge | From digital audio input circuit |
| P1.5 | RS | O | LCD display register select signal | |
| P1.6 | R/W | O | LCD display Read/Write strobe | |
| P1.7 | E | O | LCD display enable signal | |
| P3.2 | /AUXINT | INT | Interrupt from UART on falling edge | From RS-232 circuit |
| P3.3 | /FRQINT | INT | Interrupt from frequency counter on falling edge | From clock control circuit |
| P4.0 | LCD0 | I/O | LCD display data bus bit 0 | |
| P4.1 | LCD1 | I/O | LCD display data bus bit 1 | |
| P4.2 | LCD2 | I/O | LCD display data bus bit 2 | |
| P4.3 | LCD3 | I/O | LCD display data bus bit 3 | |
| P4.4 | LCD4 | I/O | LCD display data bus bit 4 | |
| P4.5 | LCD5 | I/O | LCD display data bus bit 5 | |
| P4.6 | LCD6 | I/O | LCD display data bus bit 6 | |
| P4.7 | LCD7 | I/O | LCD display data bus bit 7 | |
| P5.1 | NET_FAULT | O | ISDN fail, (loss of channel). "1" = Fault, "0" =no fault | From triple basic rate interface |
| P5.2 | LCA_DONE | I/O | "1" = LCA active after configuration. If forced low: reprogramming | From clock control circuit |
| P5.3 | LCA_RDY | I | "0" = ready , "1" = busy during configuration load | From clock control circuit |
| P5.4 | /LCA_INIT | I | "0" indicates that LCA is in power-up state and not ready | From clock control circuit |

*Table 4.1 On-Chip I/O Bits (Continued)*

| Bit | Name | I/O | Description | Source/Destination |
|---|---|---|---|---|
| P5.5 | INVENT | O | "1" signals invalid entry to the remote connector at the rear | To remote connector |
| P5.6 | REMEN | I | "1" means that remote control is enabled from the rear panel | From remote connector |
| P5.7 | /EN_LOW_FLASH | O | "0" indicates that the Flash is enabled in lower 8k | |
| P6.6 | DFDSP | I | "1" indicates data from DSP | From data exchange port |
| P6.7 | DSPRDY | I | "1" indicates DSP ready, i.e. it has read the last written byte of data | From data exchange port |

*Table 4.1 On-Chip I/O Bits (Continued)*

| Signal | Description | Range |
|---|---|---|
| /FIFOWR | Write strobe to the FIFO register | 0x00-0x1F |
| /REMRD | Read strobe to the remote control port | 0x00-0x1F |
| /KEYRD | Read strobe to the keypad encoder | 0x20-0x3F |
| /STAT1WR | Write strobe to LSB part of status port | 0x20-0x3F |
| /STAT2WR | Write strobe to MSB part of status port | 0x40-0x5F |
| /S8 | Decoded chip select signal to the LCA (QD18) | 0xE0-0xFF |
| /LEDWR | Write strobe to LED driver port | 0x60-0x7F |
| /DEXWR | Write strobe to data exchange port | 0xC0-0xDF |
| /DEXRD | Read strobe to data exchange port | 0xC0-0xDF |
| /S5 | Decoded chip select signal to the UART | 0x80-0x9F |
| /AESCS | Decoded chip select signal to the AES/EBU receiver | 0xA0-0xBF |

*Table 4.2 Decoded External I/O Selects*

### 4.2.3 Circuit Description

Fig. 4.1 shows a block diagram of the controller circuit.

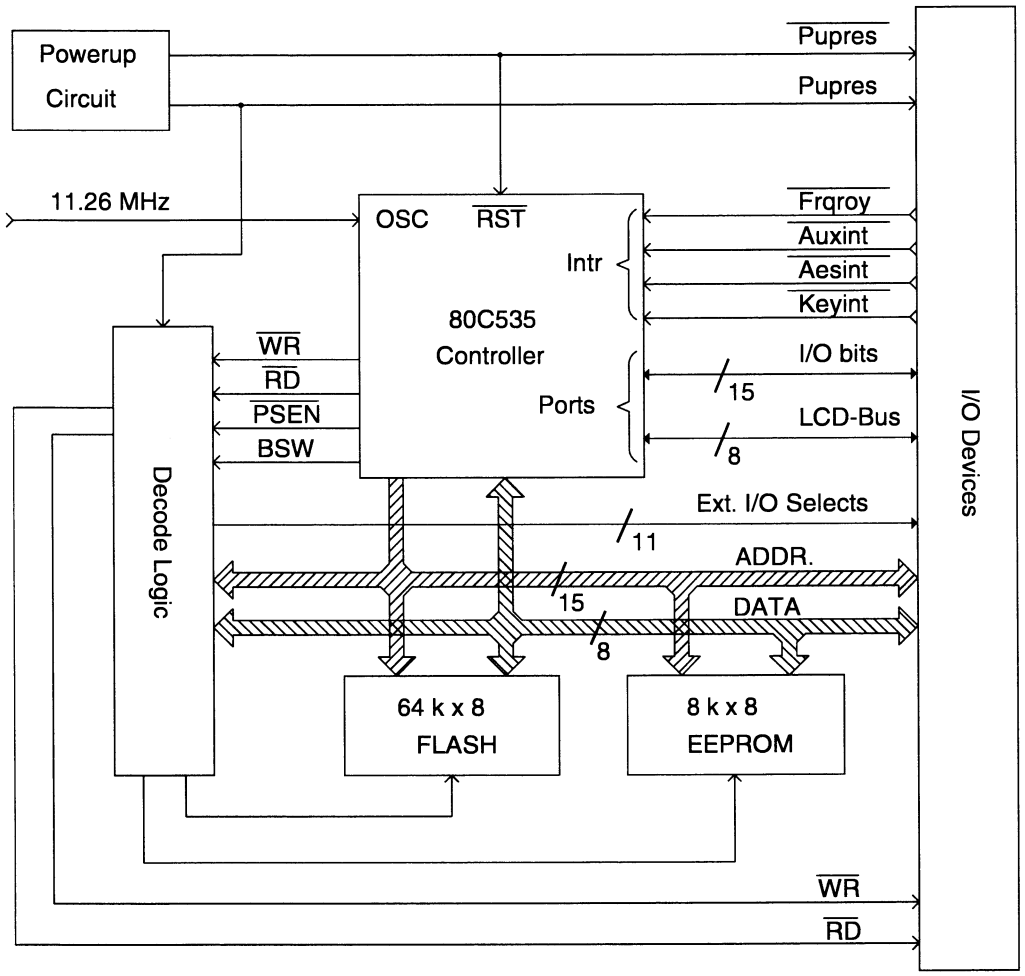


*Fig. 4.1 The Layer II Encoder Controller Circuit*

The controller consists of an 80C535 micro controller equipped with 64 kbyte external FLASH memory (QD71) and 8 kbyte external EEPROM memory (QD70). The 8 kbyte of EEPROM memory is bank switched with the top 8 kbyte of FLASH memory. When the bank switch signal (BSW) is high, the EEPROM is selected.

**If EN_LOW_FLASH = "1":**

The bottom 8 kbyte of the external memory is mapped as external I/O for data memory transfers and as FLASH memory for program memory transfers. The address decoding of the external data memory ports is handled by QD69. External data memory reads from the FLASH are disabled in the bottom 8 kbyte by signal EXMEMDIS (QD11, 12) which also serves as write protection by disabling the write strobe in the same area. During power-up the FLASH memory is write protected by QD50.

### If EN_LOW_FLASH = "0":

The bottom 8 kbyte of external memory is mapped as FLASH memory for data and program memory transfers.

The supervisory circuit (QA19) ensures a proper power-up reset pulse both to the controller and to the rest of the system.

Table 4.3 shows a memory map of the external program/data memory of the controller.

| | /EN_LOW_FLASH = "1" | | | | = "0" | |
|---|---|---|---|---|---|---|
| | **Program Memory** | | **Data Memory** | | **Data Memory** | |
| Address: | BSW="0" | BSW="1" | BSW="0" | BSW="1" | BSW="0" | BSW="1" |
| 0000-0FFF | FLASH | | I/O | | FLASH | |
| 1000-1FFF | FLASH | | I/O | | FLASH | |
| 2000-2FFF | FLASH | | | | | |
| 3000-3FFF | - | | | | | |
| 4000-4FFF | - | | | | | |
| 5000-5FFF | - | | | | | |
| 6000-6FFF | - | | | | | |
| 7000-7FFF | - | | | | | |
| 8000-8FFF | - | | | | | |
| 9000-9FFF | - | | | | | |
| A000-AFFF | - | | | | | |
| B000-BFFF | - | | | | | |
| C000-CFFF | - | | | | | |
| D000-DFFF | - | | | | | |
| E000-EFFF | 4k FLASH | $E^2$prom | 4k FLASH | $E^2$prom | 4k FLASH | $E^2$prom |
| F000-FFFF | 4k FLASH | $E^2$prom | 4k FLASH | $E^2$prom | 4k FLASH | $E^2$prom |

*Table 4.3 Controller Memory Map*

## 4.3 RS-232-C Input

### 4.3.1 General Description

The RS-232-C input is used for auxiliary data transfers inside the Layer II frames and for software updates of the codec. Possible baud rates are 300, 600, 1200, 2400, 4800 and 9600.

### 4.3.2 Circuit Description

The circuit consists of a SCC2691 UART (QD32) with a 3.6864 MHz crystal for the master clock oscillator. The UART is mapped into the external data memory of the controller, and is selected by the /S5 chip select signal at address 0x80-0x9F.

The controller handles the setup of the UART through eight internal read/write registers selected by A0-A2. When the UART has received a character, it issues an interrupt by asserting the INTR pin. When the interrupt is recognized by the controller, the received character is read from the UART, and the INTR is de-asserted.

QD33 handles level conversion from RS-232 to TTL using an internal charge pump built up around external capacitors C207 and C208.

The Request To Send signal (RTS) is passively pulled to the ON state by R154 allowing connections to equipment without RTS/CTS handshake. Additionally, signals RI, DCD and DSR are pulled to the ON state by R139, R134 and R138 allowing connections to equipment requiring these signals to be ON.

The physical connection to the RS-232-C channel is made through the 25-pole SUB-D connector (RS-232 INPUT) on the rear panel. The encoder is configured as a Data Communications Equipment (DCE) unit.

## 4.4 Alarm and Remote Control Circuits

### 4.4.1 General Description

The alarm output located on the rear panel is activated if a fault situation is detected by the controller. Examples of possible faults are ISDN faults, a missing digital audio input signal or an internal circuit fault.

The remote control function allows the encoder to be controlled from a remote location instead of from the front panel.

### 4.4.2 Circuit Description

The alarm circuit is formed by transistor Q7 and the relay K1. The relay is capable of switching up to 50 W. In an alarm situation, the controller switches Q7 off which means that the relay is released and there will be a short circuit between pins 2 and 15 and an open circuit between pins 1 and 14 in the alarm/remote connector located on the rear panel. The alarm circuit is in the alarm position when there is no power to the encoder.

The remote control function is implemented using 13 HCMOS input bits which can be set up from the alarm/remote connector located on the rear panel. Each input is pulled high by a 10 k resistor, and is therefore default set to logic "1". The bits can be read by the controller via two 8-bit input ports (QD25, QD29). The controller only reads and uses the remote information if bit REMIN is held at logic low level.

## 4.5 Front Panel

### 4.5.1 General Description

The front panel is controlled by the controller and consists of a 16-character one-line LCD display for displaying status about the setup, nine keys for controlling setup, and six LEDs for displaying information concerning alarms and operation of the encoder.

### 4.5.2 Circuit Description

Communication with the display is made through the LCD data bus (controller P4) with register select (RS), Enable (E) and read/write (R/W) signals controlled from P1 on the controller.

The circuit with Q9 and Q10 supplies the back plane light with a constant current. R123, R124, R190 and R191determine the contrast of the display.

The keys are scanned by the keypad encoder QD44 (74C922) with a scan frequency of 4 kHz (KEYCLK). If a key is pressed, the keypad encoder detects it, and after the debouncing time determined by capacitor C229, the keypad encoder generates a low to high level transition on pin 12 (KEYINT). The KEYINT signal remains high until the key is pressed or another key is pressed. While the KEYINT signal is high, a 4-bit binary code is available at pins 14 to 17. Table 4.4 shows the key codes.

The six LEDs at the front panel are controlled by the controller via an 8-bit external output port (QD31). Table 4.5 shows each bit in the LED output port.

| KEYD3-D0 | Key | KEYD3-D0 | Key |
|---|---|---|---|
| 0000 | AUX | 0101 | INPUT |
| 0001 | RATE | 0110 | MODE |
| 0010 | ↑ | 0111 | ENTER |
| 0011 | FS | 1000 | CANCEL |
| 0100 | ↓ | | |

*Table 4.4 Controller Key Codes*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | Remote | Invalid Entry | Dig. Audio Loss | Network Fault | Ext. Clock | Int. Clock |

*Table 4.5 LED Port Bit Assignment*

## 4.6 Encoder DSP

### 4.6.1 General Description

The encoder DSP handles the audio compression and forms the ISO MPEG Layer II frames. The audio samples are read from the ADC or the digital audio input circuit, and are compressed according to the output bit rate and mode, which is read from the status port. After compression of the audio, it is sent to the B-channel equalizer in the form of MPEG frames.

### 4.6.2 Circuit Description

Fig. 4.2 shows a block diagram of the encoder DSP.

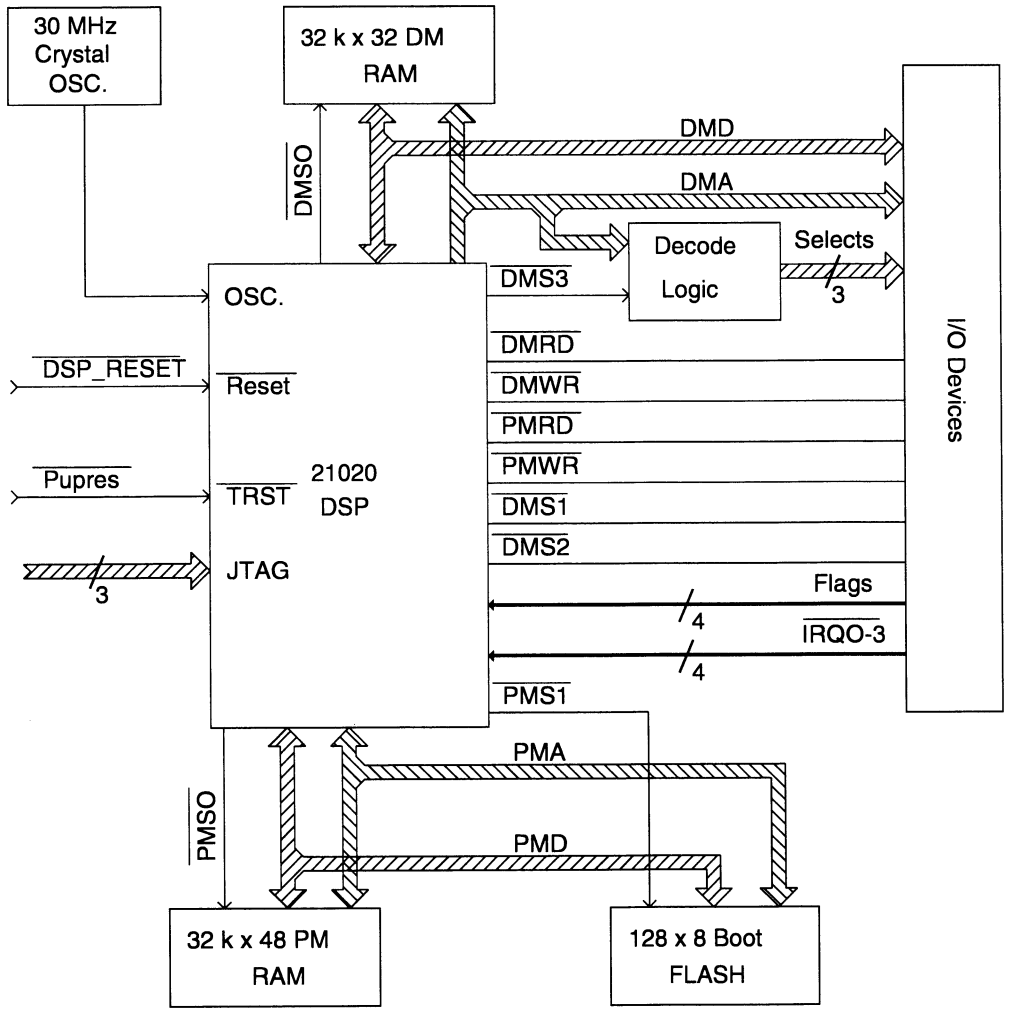


*Fig. 4.2 The Encoder DSP*

The DSP circuit consists of a 21020 floating point processor (QD59) equipped with 32kx48 program memory and 32kx32 data memory. The CPU clock is generated by a 30 MHz Dual In Line (DIL) crystal oscillator (QD60).

After power-up, the controller loads the DSP with a small boot loader program through the JTAG port (J12). Data to the DSP (JTDI) is clocked in on the rising edge of the JTCK signal.

When the loader starts running in the DSP, it loads the compression program from the 128 kbyte boot FLASH (QD45) which is mapped into program memory space. QD50 ensures write protection of the FLASH during power-up.

The signal flow in and out of the DSP is interrupt controlled using /IRQ1, /IRQ2 and /IRQ3. When data is ready from the IIS interface (ADC), the DSP receives an interrupt on /IRQ3 (/I²SINT). Similarly, data is output to the network interface when requested by an /IRQ1 or /IRQ2 interrupt from the A or B channel respectively.

QD46 decodes the internally generated select signal /DMS3 into eight sub-decoded select signals. Three of these signals (/DSEL1-DSEL3) are used to select the FIFO register, the data exchange port and the status port.

Table 4.6 shows the data memory map of the encoder DSP.

<table>
<tr><th>Addr.</th><th colspan="4">Encoder Data Memory (DMD Bus)</th></tr>
<tr><td></td><td colspan="4">39----------32 31----------24 23----------16 15----------8 7----------0</td></tr>
<tr><td>0000h<br><br>7FFFh</td><td colspan="3">32k RAM (/DMS0)</td><td rowspan="6">FREE</td></tr>
<tr><td>8000h<br>80FFh</td><td>IIS read (/DMS1)<br>PSI A write (/DMS1)</td><td colspan="2">FREE</td></tr>
<tr><td>8100h<br>8FFFh</td><td>PSI B write<br>(/DMS2)</td><td colspan="2">FREE</td></tr>
<tr><td>9000h<br>91FFh</td><td colspan="2">FREE</td><td>FIFO read<br>(/DSEL1)</td></tr>
<tr><td>9200h<br>93FFh</td><td colspan="2">FREE</td><td>DEX rd/wr<br>(/DSEL2)</td></tr>
<tr><td>9400h<br>95FFh</td><td>FREE</td><td colspan="2">STATUS rd (/DSEL3)</td></tr>
<tr><td>9600h<br>97FFh</td><td colspan="4">DSEL4<br>(free)</td></tr>
<tr><td>9800h<br>9AFFh</td><td colspan="4">DSEL5<br>(free)</td></tr>
<tr><td>9A00h<br>9BFFh</td><td colspan="4">DSEL6<br>(free)</td></tr>
<tr><td>9C00h<br>9DFFh</td><td colspan="4">DSEL7<br>(free)</td></tr>
<tr><td>9E00h<br>9FFFh</td><td colspan="4">DSEL8<br>(free)</td></tr>
</table>

*Table 4.6 Encoder DSP Data Memory Map*

## 4.7 IIS Interface

### 4.7.1 General Description

The IIS interface is used to convert the 32-bit serial data (IIS format) from the analog or digital audio input into a 16-bit parallel data format. Upon interrupt, the DSP reads the 16-bit audio samples for left or right channel from the IIS interface.

### 4.7.2 Circuit Description

The serial data is clocked into the 16-bit serial-to-parallel shift register (QD10, QD11) on the rising edge of CLK. When the 16 bits of audio data are clocked into the register they are clocked to the output register in parallel form by a register clock signal at QD8,9. This signal is used in negated form to interrupt the DSP indicating that an audio sample is ready (QD8,8).

The DSP is interrupted separately from left and right channel samples, and hence the interrupt frequency is twice the sample frequency. After each interrupt, QD15,9 indicates whether it was a left or right sample which caused the interrupt ("0" = left).

QD13 serves as a "count 16" counter and ensures that only the 16 MSB bits of the 32-bit serial data is used for each channel.

## 4.8 Parallel To Serial Interface

### 4.8.1 General Description

The parallel to serial interface is used to shift the DSP-generated MPEG frames in serial to the B-channel equalizer board. The circuit is timed by the Layer II clock and automatically interrupts the DSP when 16 new bits are needed. The DSP loads the corresponding circuit in parallel upon an interrupt.

### 4.8.2 Circuit Description

The MPEG frames are shifted serially out of registers QD42 and QD43 on the falling edge of the clock signal CLOCK_A (Layer II clock from the B-channel equalizer board). The counter QD40 counts 16 clock periods and triggers the parallel load circuit QD35 to generate a load pulse of one half-bit time duration to the registers. This load pulse transfers the current 16-bit word from the input holding register of QD42 and QD43 to the output shift register. The first bit of the word is shifted out on the next falling edge of the CLOCK signal.

The counter output (QD40, 6) also serves as an interrupt to the DSP indicating that a new 16-bit word is needed. When the DSP acknowledges this interrupt, it writes the new word to the input holding register of QD42 and QD43 through the gate QD41,6.

## 4.9 Common DSP and Controller Ports

### 4.9.1 General Description

The controller and the DSP communicate through three ports. A FIFO is used to buffer auxiliary data from the RS-232 input, before they are inserted in the MPEG frames by the DSP. Various information is exchanged between the two processors through a data exchange port (DEX). Additionally, status and setup information is signaled to the DSP from the controller via a status port.

### 4.9.2 FIFO Circuit Description

The FIFO (QD28) is used to buffer auxiliary data from the RS-232 input so that the DSP can read data in blocks for each MPEG frame generated. The controller writes characters to the FIFO as they are received from the UART. The DSP monitors the empty flag (QD28 pin 21) once for each MPEG frame generated. If the empty flag is high, there is data from the auxiliary input and the DSP empties the FIFO by reading it until the flag goes low. The FIFO internal read/write pointers are reset at power-up by the signal /PUPRES at pin 22.

### 4.9.3 Data Exchange Port Circuit Description

The data exchange port consists of QD47, QD48 and QD49. QD48 and QD49 are used as an 8-bit bi-directional port with input registers and output enable. QD47 serves as a control circuit for the four handshake signals: Data from controller (DFCON), Controller ready (CONRDY), Data from DSP (DFDSP) and DSP ready (DSPRDY).

When the DSP writes data to the controller, the write strobe sets QD47,5 high indicating DFDSP to the controller. Likewise, QD47,9 is set high to indicate DFCON when the controller writes to the data exchange port. When the receiving processor reads the port, the corresponding bit goes low again and indicates DSPRDY or CONRDY.

### 4.9.4 STATUS Port Circuit Description

The status port is a 16-bit port formed by QD24, QD27 and QD30. The port is mapped as two 8-bit ports at the controller end and as one 16-bit port at the DSP end.

Status written from the controller to the LSB part is constantly available to other circuits in the system. The same bits are available to the DSP through the tristate buffer QD27. The MSB part is only available to the DSP.

Tables 4.7 to 4.9 show the status port bits as seen from the DSP data memory data bus (DMD).

| DMD 22 | DMD 12 | DMD 11 | FS | DMD 10 | Input | DMD 9 | DMD 8 | Emphasis |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Reserved | 0 | Analog | 0 | 0 | None |
| 0 | 0 | 1 | 16.0 kHz | 1 | Digital | 0 | 1 | 50/15 us |
| 0 | 1 | 0 | 22.05 kHz | | | 1 | 0 | Reserved |
| 0 | 1 | 1 | 24.0 kHz | | | 1 | 1 | J.17 |
| 1 | 0 | 0 | Reserved | | | | | |
| 1 | 0 | 1 | 32.0 kHz | | | | | |
| 1 | 1 | 0 | 44.1 kHz | | | | | |
| 1 | 1 | 1 | 48.0 kHz | | | | | |

*Table 4.7 STATUS Port Bit Definitions*

| DMD15 | DMD14 | DMD13 | Aux. Rate |
|---|---|---|---|
| 0 | 0 | 0 | No aux data |
| 0 | 0 | 1 | 300 baud |
| 0 | 1 | 0 | 600 baud |
| 0 | 1 | 1 | 1200 baud |
| 1 | 0 | 0 | 2400 baud |
| 1 | 0 | 1 | 4800 baud |
| 1 | 1 | 0 | 9600 baud |

*Table 4.8 STATUS Port Bit Definitions*

| DMD 21 | DMD 20 | Mode | DMD 19 | DMD 18 | DMD 17 | DMD 16 | Network Bit Rate |
|---|---|---|---|---|---|---|---|
| 0 | 0 | Stereo | 0 | 0 | 0 | 0 | No bit clock |
| 0 | 1 | Joint Stereo | 0 | 0 | 0 | 1 | 56 kHz |
| 1 | 0 | Dual Channel | 0 | 0 | 1 | 0 | 64 kHz |
| 1 | 1 | Single Channel | 0 | 1 | 0 | 0 | 112 kHz |
| | | | 0 | 1 | 0 | 1 | 128 kHz |
| | | | 0 | 1 | 1 | 0 | 192 kHz |
| | | | 0 | 1 | 1 | 1 | 256 kHz |
| | | | 1 | 0 | 0 | 0 | 320 kHz |
| | | | 1 | 0 | 0 | 1 | 384 kHz |

*Table 4.9 STATUS Port Bit Definitions*

## 4.10 Analog Audio Input

### 4.10.1 General Description

The Analog Audio Input can digitize up to two analog audio input signals at a rate equal to 64 times over-sampling relative to 32, 44.1 and 48 kHz. The resulting left and right channel samples are presented as a serial data stream associated with a bit clock and a word select signal defining the boundaries of each sample.

### 4.10.2 Jumper Settings

The input impedance can be set to 600 Ω or to high impedance (>25 kΩ) as shown in Table 4.10.

Fig. 4.10 shows the diagram of the location of the adjustable components in the encoder.

| Input Impedance | JP3 Left Channel | JP10 Right Channel |
|---|---|---|
| >25 kΩ | 1-2 | 1-2 |
| 600 Ω[a)] | 2-3 | 2-3 |

*Table 4.10 Analog Audio Inputs*

a. Factory setting

The clipping level can be set to -3, 0, +3, +6, +9, +12, +15, +18 or +21 dBu to meet different requirements for average program levels and head rooms.

| Clipping Level | TP8 | TP7 | TP6 | TP5 | TP9 | TP10 | TP12 | TP11 |
|---|---|---|---|---|---|---|---|---|
| 21 dBu | 2-3 | 2-3 | 1-2 | 2-3 | 2-3 | 2-3 | 1-2 | 2-3 |
| 18 dBu | 2-3 | 2-3 | 2-3 | 1-2 | 2-3 | 2-3 | 2-3 | 1-2 |
| 15 dBu[a)] | 2-3 | 2-3 | 2-3 | 2-3 | 2-3 | 2-3 | 2-3 | 2-3 |
| 12 dBu | 2-3 | 1-2 | 1-2 | 2-3 | 2-3 | 1-2 | 1-2 | 2-3 |
| 9 dBu | 2-3 | 1-2 | 2-3 | 1-2 | 2-3 | 1-2 | 2-3 | 1-2 |
| 6 dBu | 2-3 | 1-2 | 2-3 | 2-3 | 2-3 | 1-2 | 2-3 | 2-3 |
| 3 dBu | 1-2 | 2-3 | 1-2 | 2-3 | 1-2 | 2-3 | 1-2 | 2-3 |
| 0 dBu | 1-2 | 2-3 | 2-3 | 1-2 | 1-2 | 2-3 | 2-3 | 1-2 |
| -3 dBu | 1-2 | 2-3 | 2-3 | 2-3 | 1-2 | 2-3 | 2-3 | 2-3 |

*Table 4.11 Encoder Clipping Level*

a. Factory setting

### 4.10.3 Interfaces

| Signal | Description |
|---|---|
| | Left channel analog audio input from the rear panel |
| | Right channel analog audio input from the rear panel |
| FSEL0 | Sample frequency select (LSB) from the controller |
| FSEL1 | Sample frequency select (MSB) from the controller |

*Table 4.12 Input/Output Lines, Analog Audio Input*

| Signal | Description |
|---|---|
| 8192 kHz | Sample frequency input from the clock control circuit |
| 6144 kHz | Sample frequency input from the clock control circuit (not used in current design) |
| 11289.6 kHz | Sample frequency input from the clock control circuit |
| 12288 kHz | Sample frequency input from the clock control circuit |
| CLK | Bit clock output to the Layer II encoder, audio monitor and digital audio input |
| WS | Sample identifier output to the Layer II encoder, audio monitor and digital audio input |
| DATA | Serial data output comprising both left and right samples to the digital audio input |
| 256XFS | A 256 times the sample frequency clock signal used as master clock to the audio monitor DAC |
| PUPRES | Power-up reset of the ADC from the controller |

*Table 4.12 Input/Output Lines, Analog Audio Input*

### 4.10.4 Circuit Description

Fig. 4.3 shows a block diagram of the analog audio input circuit.

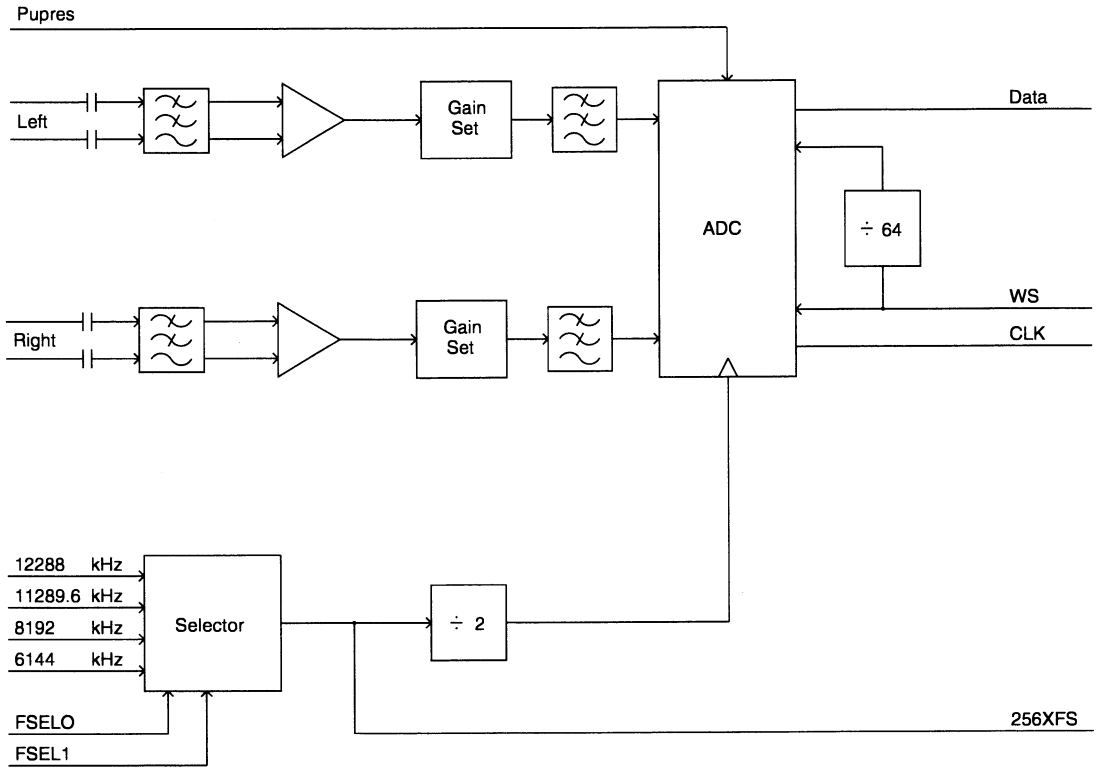


*Fig. 4.3 The Analog Audio Input Circuit*

The analog input circuits used for the left and right audio input are identical. The inputs are DC blocked and lowpass-filtered by a passive filter with a cut-off frequency around 250 kHz. Next the signals are transformed into single-ended signals by a differential amplifier and passed to the gain section. In the gain section, the signals are amplified to give a clipping level as set by the jumpers, and they are lowpass-filtered to remove out-of-band noise, before they are converted to digital form in the audio ADC.

The clock control circuit supplies three clock frequencies, one for each sample rate, and the controller signals which of the three rates has been enabled on FSEL0 and FSEL1. The enabled clock frequency is divided by 2 to give a 50 % duty cycle, and is fed to the audio ADC which samples both audio inputs at every second clock cycle.

When 16, 22.05 or 24 kHz sampling is required, the conversion from analog to digital takes place at the full 32, 44.1 or 48 kHz. The Layer II encoder decimates the audio samples by 2 to divide the sample rate by 2 prior to the Layer II encoding.

The audio ADC supplies a sample clock (input clock divided by 2) which is divided by 64 to supply a left-right word select signal to the ADC. The word select signal, the data and bit clock output are transferred to the digital audio input circuit.

### 4.10.5 Adjustments

For the analog audio input circuit only the analog audio gain can be adjusted. Fig. 4.10 shows the diagram of the location of the adjustable components in the encoder.

The adjustments require the use of the following:

- A 1 kHz sine wave source with an output level of approximately +9 dBu.
- A DVM capable of a 1 kHz AC voltage measurements.
- An RE 663 ISDN Layer II Decoder.
- An ISDN circuit to connect the RE 662 and RE 663.

#### Left Channel Gain Adjustment

1. Connect the RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder to ISDN and establish a minimum of 4 B-channels.
2. Make sure that the analog audio gain in the RE 663 ISDN Layer II Decoder is aligned.
3. Apply a 1 kHz sine wave with an amplitude of approximately 9 dBu at the left channel input connector.
4. Measure the actual applied level of the sine wave on the input connector using a DVM.
5. Connect the DVM to the left channel output of the RE 663 ISDN Layer II Decoder, and terminate the output with 600 Ω.
6. Adjust R28, until the DVM reads the same value as measured on the input to the encoder ±0.05 dB.

#### Right Channel Gain Adjustment

1. Connect the RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder to ISDN and establish a minimum of 4 B-channels.
2. Make sure that the analog audio gain in the RE 663 ISDN Layer II Decoder is aligned.
3. Apply a 1 kHz sine wave with an amplitude of approximately 9 dBu at the right channel input connector.
4. Measure the actual applied level of the sine wave on the input connector using a DVM.
5. Connect the DVM to the right channel output of the RE 663 ISDN Layer II Decoder, and terminate the output with 600 Ω.

6. Adjust R25, until the DVM reads the same value as measured on the input to the encoder ±0.05 dB.

## 4.11 Audio Monitor

### 4.11.1 General Description

The audio monitor provides analog headphone monitoring capability of the audio input signals. The monitor is accessible at the front panel along with a volume control.

As the monitor is driven by a DAC which converts the digital audio samples into analog signals, the monitor carries analog signals for conventional headphone monitoring even when the digital audio input is used.

### 4.11.2 Interfaces

| Signal | Description |
|---|---|
| DATA | Serial data input from the digital audio input circuit, comprising both left and right channel samples |
| WS | Sample identifier from the digital audio input circuit |
| CLK | Bit clock from the digital audio input circuit |
| 256XFS | A 256 times the sample frequency clock from the analog audio input |
| EMPH0 | Control signal (LSB) from the controller |
| EMPH1 | Control signal (MSB) from the controller |
| LEFT | Left channel monitor output |
| RIGHT | Right channel monitor output |

*Table 4.13 Input/Output Lines, Audio Monitor*

### 4.11.3 Circuit Description

Fig. 4.4 shows a block diagram of the audio monitor circuit.

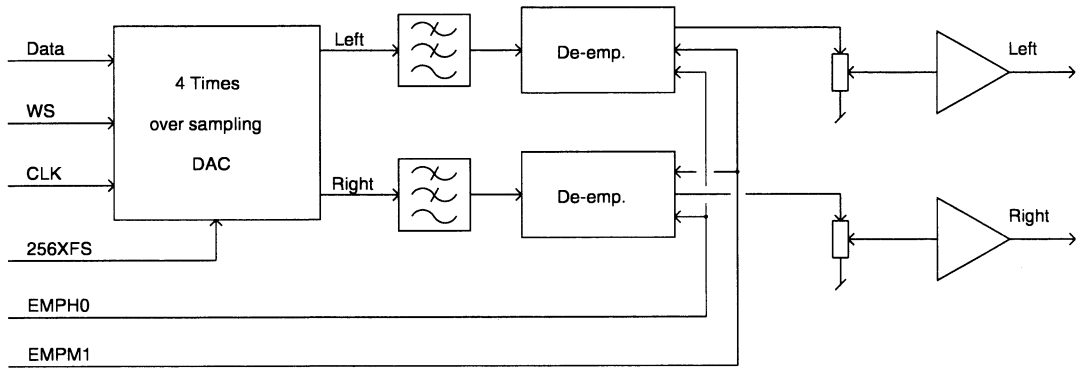


*Fig. 4.4 The Audio Monitor Circuit*

The serial data input, bit clock and word select signals from the digital audio input circuit are fed to a four times over-sampling DAC with a built-in interpolation filter. The DAC is operated on the 256XFS clock from the analog audio input circuit.

The left and right analog audio output from the DAC are lowpass-filtered to remove sampling mirrors by two passive analog filters. After filtering, the signals are de-emphasized according to the ITU-T J.17 or the 50/15 µs specifications when commanded by the EMPH0 and EMPH1 signals from the controller.

Despite the fact that the analog audio input signals to the RE 662 ISDN Layer II Encoder are not pre-emphasized, it is necessary to allow de-emphasis as the digital audio input signal can be comprised of audio signals that have been emphasized according to the above specifications.

The de-emphasis networks are implemented using an inverting operational amplifier circuit with the de-emphasis network in its feedback loop. Figs. 4.5 and 4.6 show the amplitude transfer function of the de-emphasis networks.

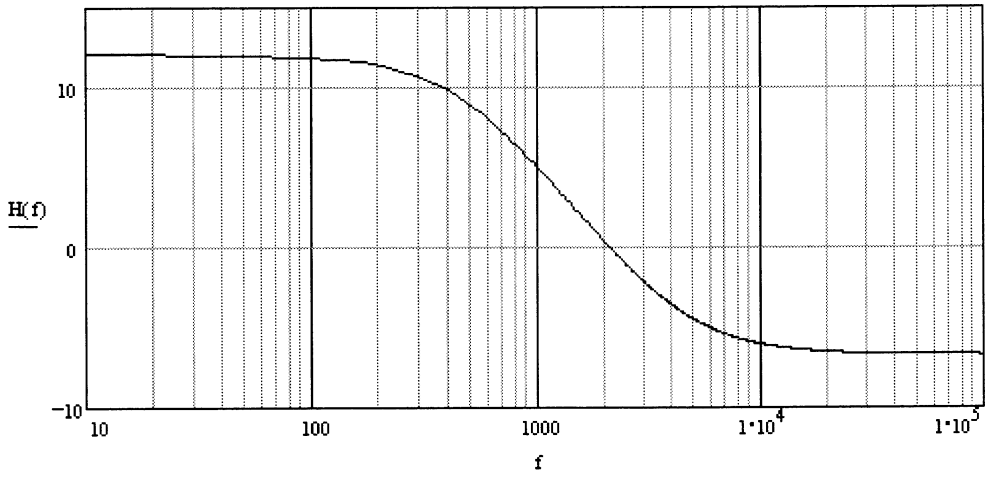


*Fig. 4.5 ITU-T J.17 De-emphasis*

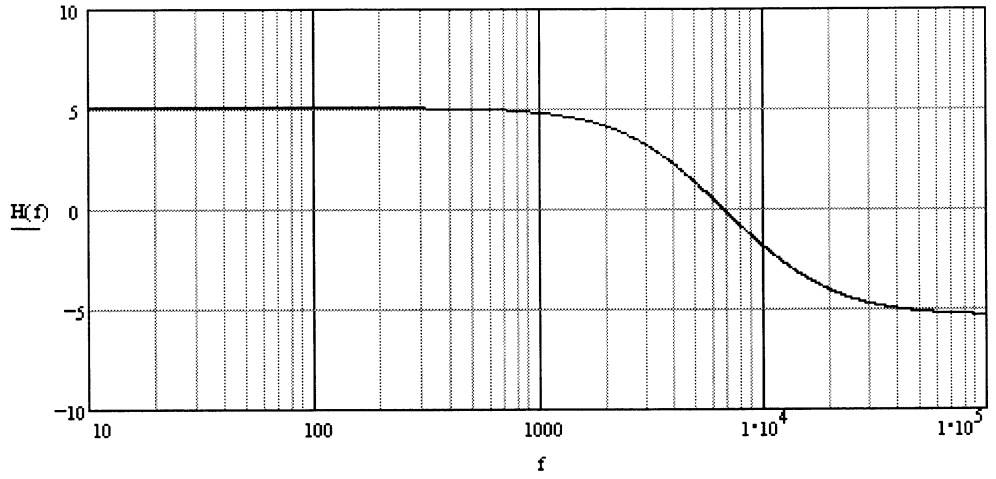


*Fig. 4.6 50/15 μs De-emphasis*

After de-emphasis, the audio signals are level adjusted by the front panel potentiometer and buffered to drive the stereo headphone output.

## 4.12 Clock Control Circuit

### 4.12.1 General Description

The clock control circuit repeatedly measures the frequency of the clock input from the B-channel equalizer board and forwards the readings to the controller. The controller uses the clock frequency measurement to determine the transmission rate, and hence controls that Layer II frames are encoded accordingly. Secondly, the clock input is used as reference frequency for PLLs generating the three audio sample frequencies.

### 4.12.2 Interfaces

| Signal | Description |
|---|---|
| CLOCK_A | Clock to collect data from the Layer II encoder to be transmitted to the B-channel equalizer board |
| CLOCK_B | This signal is unused in this configuration |
| DATA_A | Data from the Layer II encoder to be transmitted to the B-channel equalizer board |
| DATA_B | This signal is unused in this configuration |
| 6144 kHz | This signal is unused in this configuration |
| 8192 kHz | Sample frequency output to the analog audio input circuit |
| 11289.6 kHz | Sample frequency output to the analog audio input circuit |
| 12288 kHz | Sample frequency output to the analog audio input circuit |
| AD0;7 | Bi-directional data bus to controller |
| WR | Write control signal from the controller |
| RD | Read control signal from the controller |
| S8 | Chip enable signal from the controller |
| A0 | Address bit from the controller |
| PUPRES | Power-up reset signal from the controller |

*Table 4.14 Input/Output Lines, Clock Control*

| Signal | Description |
|---|---|
| LCA_DONE | Control signal to the controller confirming that software has been down loaded after power-up |
| FRQRDY | Control signal to the controller, clearing for a new clock frequency measure |
| LCA_RDY | Output signal to the controller signaling ready for next data byte during configuration after power-up |
| LCA_INIT | Output signal to the controller signaling ready to start configuration after power-up |
| KEYCLK | A 4 kHz clock output to the keyboard driver |

*Table 4.14 Input/Output Lines, Clock Control (Continued)*

### 4.12.3 Circuit Description

Fig. 4.7 shows a block diagram of the clock control circuit.

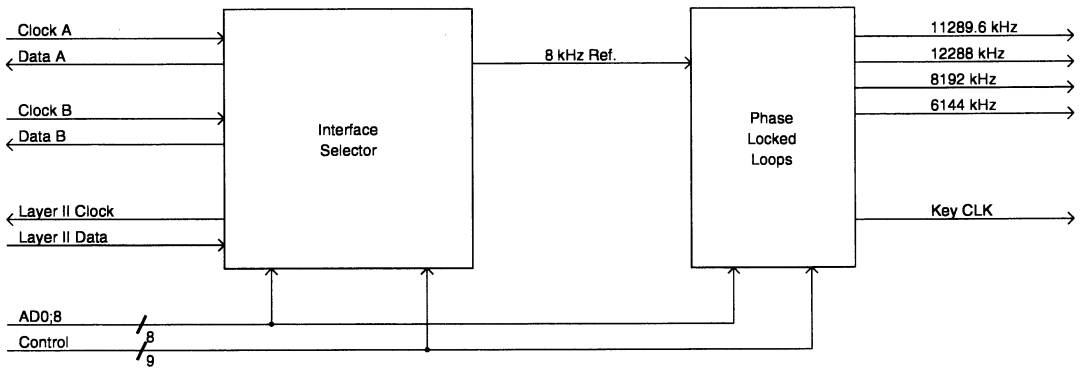


*Fig. 4.7 The Clock Control Circuit*

The clock control circuit is designed in a large Logic Cell Array comprising all the clock selectors, the frequency counter and divider circuitry for the phase locked loops. The block diagram above is intended to give the reader an understanding of the clock control circuit rather than reflecting the actual implementation (which can be seen in the schematic diagram).

The interface selector circuit, supervised by the controller, sequentially measures the clock input frequency. The input clock signal is divided by M to give an 8 kHz reference signal to which a 8,192 kHz VCXO is locked. The locked 8,192 kHz clock (the sample frequency output for 32 kHz sampling) is divided by 4 to provide a 2,048 kHz reference signal to lock a 12,288 kHz VCO (the sample frequency output for 48 kHz sampling).

Finally, the 8,192 kHz reference clock is divided by 320 giving a 25.6 kHz reference signal for locking a 11,289.6 kHz VCO (the sample frequency output for 44.1 kHz sampling).

### 4.12.4 Adjustments

Fig. 4.10 shows a diagram of the location of the adjustable components in the encoder. For the clock control circuit the following adjustments can be made:

The adjustments require the use of the following:

- A frequency counter with an accuracy better than 10 ppm at 8,192 kHz.
- A DVM or an oscilloscope.

#### Internal Reference Adjustment

1. Short-circuit TP 15.
2. Connect the frequency counter to TP 1.
3. Tune L29 until the frequency counter reads 8,192,000 Hz. ±40 Hz.
4. Remove the short-circuit on TP 15

#### 12 MHz PLL Adjustment

1. Short-circuit TP 15.
2. Connect the DVM or oscilloscope to TP 4.
3. Tune L15 until the DC voltage in TP 4 is 8 V ±0.5 V.
4. Remove the short-circuit on TP 15.

#### 11 MHz PLL Adjustment

1. Short-circuit TP 15.
2. Connect the DVM or oscilloscope to TP 3.
3. Tune L13 until the DC voltage in TP 3 is 8 V ±0.5V.
4. Remove the short-circuit on TP 15.

## 4.13 Digital Audio Input Option

### 4.13.1 General Description

The digital audio input can decode a digital audio input signal according to the AES/EBU or S/PDIF specification. The audio samples are extracted from the input and converted into a form synchronized to the transmission bit rate (that is, the sample frequency used to convert the analog audio inputs).

The control information contained within the digital signal is decoded, and is transferred to the controller which configures the digital audio receiver upon power-up.

### 4.13.2 Jumper Settings

To cope with either AES/EBU or S/PDIF formats, the jumpers JP1 and JP2 should be set as shown in Table 4.15. Fig. 4.10 shows a diagram of the location of the adjustable components in the encoder.

| Digital Audio Input | JP1 | JP2 |
|---|---|---|
| AES/EBU[a)] | 1-2 | 1-2 |
| S/PDIF | 2-3 | 2-3 |

*Table 4.15 Digital Audio Inputs*

a. Indicates the default setting from RE TECHNOLOGY AS.

### 4.13.3 Interfaces

| Signal | Description |
|---|---|
| | Digital audio input from the rear panel |
| INT | Interrupt to the controller signaling a change in the digital audio input |
| Control | Chip enable and read-write control from the controller |
| ADR | 5-bit parallel address bus from the controller |
| AD | 8-bit parallel bi-directional data bus from the controller |
| 30 MHz | Master clock from the Layer II encoder |

*Table 4.16 Input/Output Lines, Digital Audio Input*

| Signal | Description |
|---|---|
| WS | Sample identifier from the analog audio input |
| CLK | Bit clock from the analog audio input |
| DATA | Serial data signal comprising both left and right samples from the analog audio input |
| AN/DIG | Analog-digital audio input select signal from the controller |
| DATA | Serial data signal from the controller, comprising left and right samples from the analog input or the digital input |

*Table 4.16 Input/Output Lines, Digital Audio Input*

### 4.13.4 Circuit Description

Fig. 4.4 shows a block diagram of the digital audio input circuit.

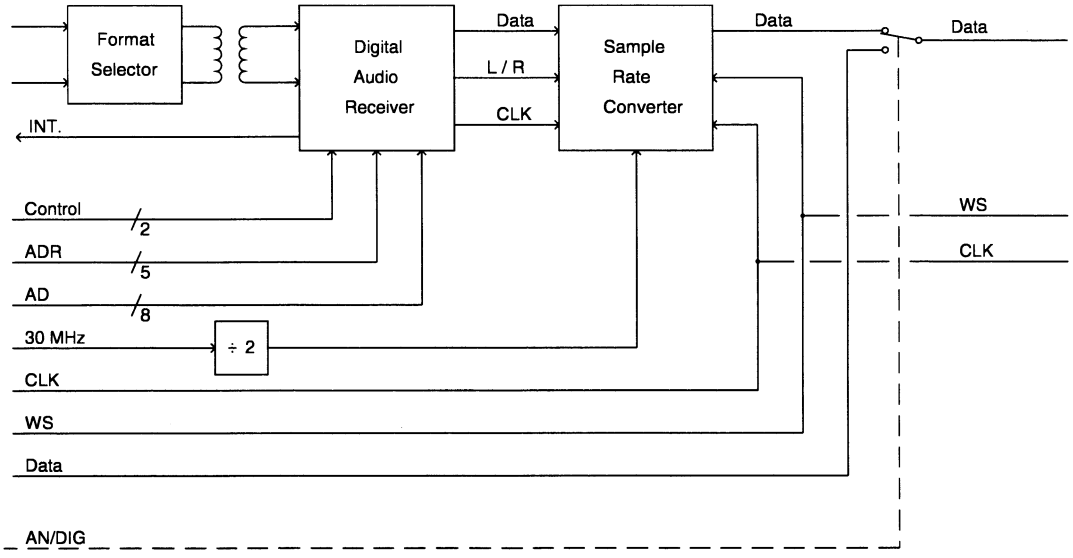


*Fig. 4.8 The Digital Audio Input Circuit*

The digital input signal enters the format selector where impedance and single-ended operation for the S/PDIF format are set. Then the signal passes through a transformer providing a galvanic separation of input from the connected digital audio source, before the signal enters the digital audio receiver.

The digital audio receiver is configured and controlled by the controller using the two control signals and the five address bits. The controller can both write (configure) and read (control) the digital audio decoder by the 8-bit data bus. The digital audio receiver locks to the incoming data signal and extracts the audio samples which are stored in the sample rate converter. The control information signaling sample frequency and possible pre-emphasis are read by the controller and used as input to the Layer II encoder block and the audio monitor.

The sample rate converter receives a 15 MHz master clock from the 30 MHz Layer II encoder DSP clock via a divide by two circuit. The input to the sample rate converter is input bit clock, input word select and input serial data from the digital audio receiver and output bit clock and output word select from the analog audio input circuit. The output bit clock and word select read the samples as a serial data stream and feed it to the input selector.

The controller enables either the serial data signal from the sample rate converter or from the analog audio input by the AN/DIG control signal.

The output data signal associated with word select and bit clock are routed to the Layer II encoder and to the audio monitor.

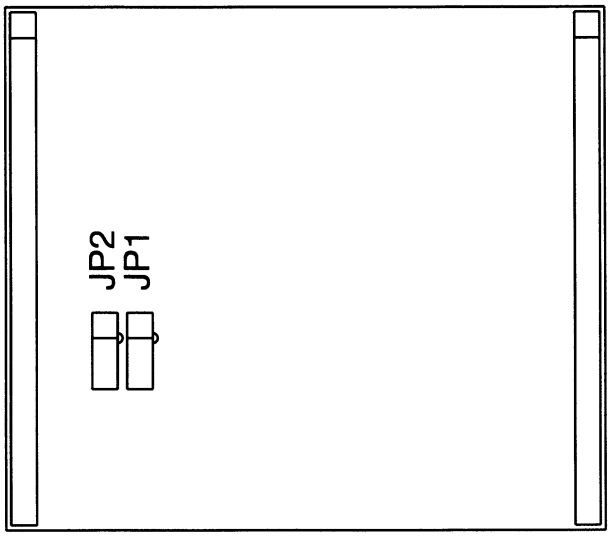


*Fig. 4.9 Adjustment points, Digital Audio Input Option*

## 4.14 Adjustable Components

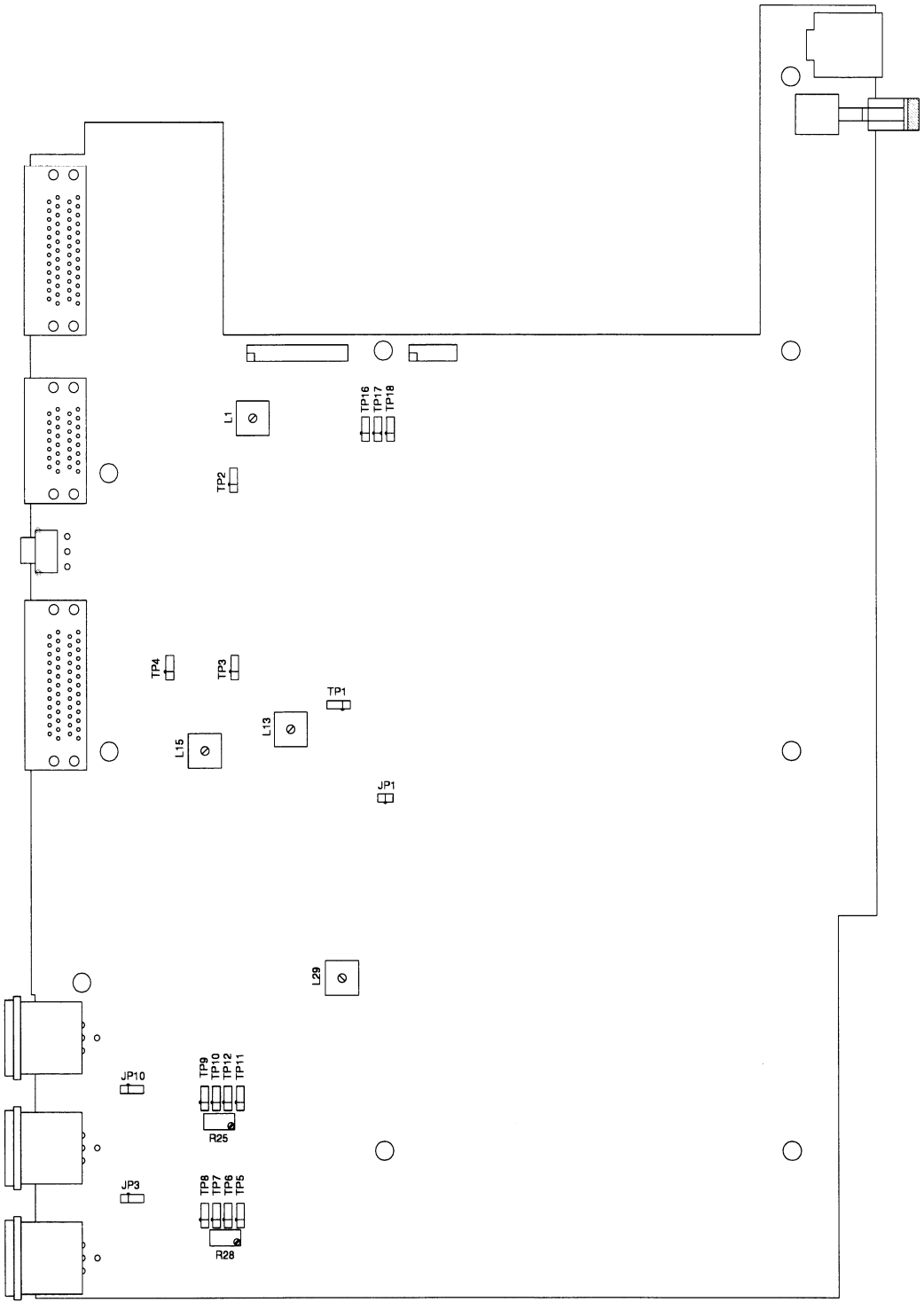


*Fig. 4.10 Adjustable Components in the Encoder Circuits*

# 5. B-channel Equalizer Circuit

This chapter describes and shows the block diagrams for the B-channel equalizer circuits.

A diagram of the locations of the adjustable components in the B-channel equalizer is shown in Chapter 5.9.

## 5.1 Status Port

### 5.1.1 General Description

The status port is 32 bits wide and works as an interface between the triple basic rate interface and the signal processing circuit of the B-channel equalizer signaling the status of each ISDN B-channel.

The triple basic rate interface updates the port whenever the status of any B-channel changes caused by a call or a disconnect. When the port has been updated, the signal processing circuit is interrupted. Being interrupted, the signal processing circuit reads the port and configures the operation of the B-channel equalizer accordingly.

### 5.1.2 Jumper Settings

The B-channel equalizer can be configured to "split" a Layer II encoded signal to be transmitted via the ISDN B-channels, or to "combine" Layer II data received from the ISDN B-channels into a serial Layer II signal.

In an RE 662 ISDN Layer II Encoder, the "split" function is always enabled feeding the ISDN B-channels with data for transmission. The "combine" function is only enabled when the return feed (from decoder to encoder) of ISDN is also used for Layer II transmission.

In an RE 663 ISDN Layer II Decoder the "combine" function is always enabled, feeding the Layer II decoder board with a restored serial Layer II data signal. The "split" function is only enabled when the return feed (from decoder to encoder) of ISDN is also used for Layer II transmission.

| Function of B-channel Equalizer | SP 1 | SP 2 |
|---|---|---|
| Split function only (RE 662 Encoder) | Open | 1 - 2 |
| Combine function only (RE 663 Decoder) | 1 - 2 | Open |
| Both split and combine function (both RE 662 and RE 663) | Open | Open |

*Table 5.1 Function of the B-channel Equalizer*

### 5.1.3 Interfaces

| Signal | I/O | Description |
|---|---|---|
| A0;7 | I | 8 bits address bus from the triple basic rate interface |
| CS1 | I | Address select signal from the triple basic rate interface |
| D0;7 | I | 8 bits data bus from the triple basic rate interface |
| IOWR | I | Memory write strobe from the triple basic rate interface |
| RESET | I | Power up reset from the triple basic rate interface |
| STAT1 | I | Read strobe triple basic rate interface |
| DMD8;39 | O | 32 bits data bus from the signal processing circuit |
| STINT | O | Interrupt signal to the signal processing circuit |
| STFLAG | O | Not used in current design |
| PUPRES | O | Reset signal to the signal processing circuit |

*Table 5.2 Input/Output Lines, Status Port*

### 5.1.4 Circuit Description

Fig. 5.1 shows a block diagram of the status port.

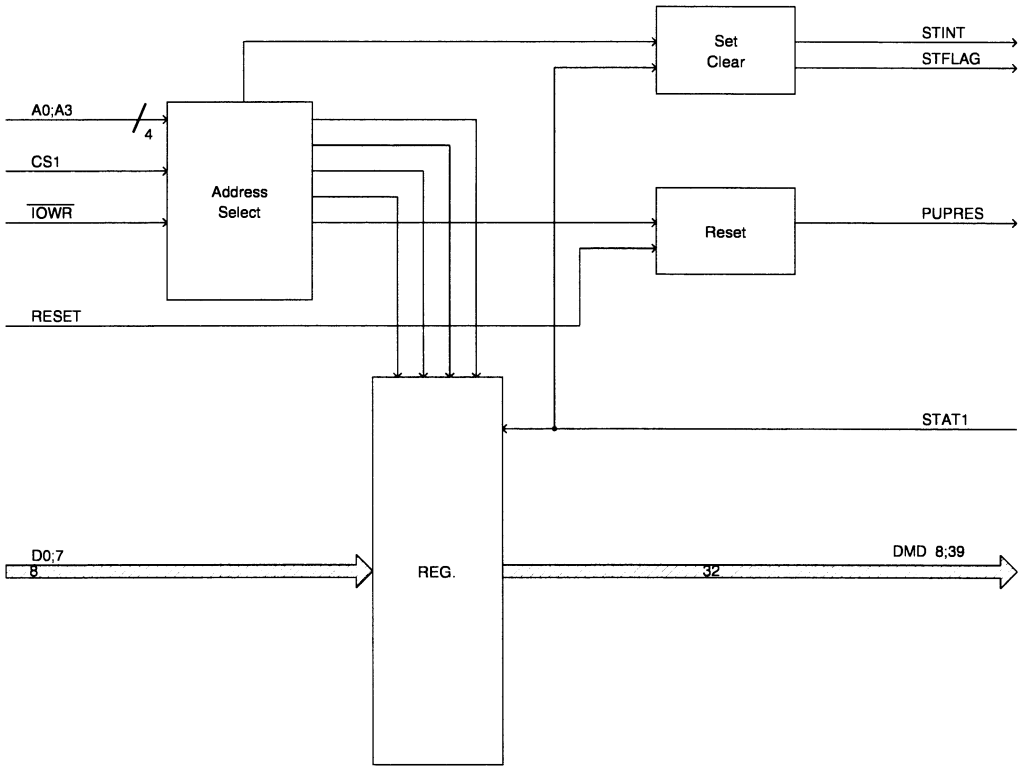


*Fig. 5.1 The Status Port*

The status port is memory mapped into both the triple basic rate interface controller and the memory of the signal processing circuit, allowing the triple basic rate interface to write to the port and the signal processing circuit to read it when interrupted by STINT.

As the data bus from the triple basic rate interface is 8 bits wide, and a status message is 32 bits wide, the status port is formed by four 8-bit registers in parallel.

The format of the status message is shown in Table 5.3

| Status Port Bit | Description |
|---|---|
| DMD8 | B-channel A is enabled to transmit/receive data when low |
| DMD9 | B-channel B is enabled to transmit/receive data when low |
| DMD10 | B-channel C is enabled to transmit/receive data when low |
| DMD11 | B-channel D is enabled to transmit/receive data when low |
| DMD12 | B-channel E is enabled to transmit/receive data when low |

*Table 5.3 Status Message Format*

| Status Port Bit | Description |
|---|---|
| DMD13 | B-channel F is enabled to transmit/receive data when low |
| DMD14 | The rate of B-channel A is 64 kbit/s when low, else 56 kbit/s |
| DMD15 | The rate of B-channel B is 64 kbit/s when low, else 56 kbit/s |
| DMD16 | Sequence number for B-channel A, LSB |
| DMD17 | Sequence number for B-channel A |
| DMD18 | Sequence number for B-channel A, MSB |
| DMD19 | Sequence number for B-channel B, LSB |
| DMD20 | Sequence number for B-channel B |
| DMD21 | Sequence number for B-channel B, MSB |
| DMD22 | Unused |
| DMD23 | Unused |
| DMD24 | Sequence number for B-channel C, LSB |
| DMD25 | Sequence number for B-channel C |
| DMD26 | Sequence number for B-channel C, MSB |
| DMD27 | Sequence number for B-channel D, LSB |
| DMD28 | Sequence number for B-channel D |
| DMD29 | Sequence number for B-channel D, MSB |
| DMD30 | Unused |
| DMD31 | Unused |
| DMD32 | Sequence number for B-channel E, LSB |
| DMD33 | Sequence number for B-channel E |
| DMD34 | Sequence number for B-channel E, MSB |
| DMD35 | Sequence number for B-channel F, LSB |
| DMD36 | Sequence number for B-channel F |
| DMD37 | Sequence number for B-channel F, MSB |
| DMD38 | Combine function enabled when high |
| DMD39 | Split function enabled when high |

*Table 5.3 Status Message Format (Continued)*

Upon power-up the STINT signal is cleared. The triple basic rate interface then initializes the port by writing "no B-channels enabled", "rates of channels A and B are 64 kbit/s" and "all channels have sequence number zero". This forces the B-channel equalizer into an idle state. When a call is performed (or received), and the called B-channels are established, the triple basic rate interface updates the status port accordingly to signal which B-channels have been established and their respective sequence numbers. Having updated all four 8-bit registers in the port, the signal processing circuit is interrupted and reads the port. By reading the port, the interrupt signal is cleared. This enables the port for the next status update.

## 5.2 Signal Processing Circuit

### 5.2.1 General Description

The signal processing circuit is based on a DSP. The DSP interfaces to the ISDN B-channels, a Layer II encoder and a Layer II decoder by memory mapped data ports. When a ports needs service (to be read or written to) the DSP is interrupted.

### 5.2.2 Jumper Settings

The circuit contains four solder points SP 9, SP 10, SP11 and SP 12, which all need to be connected 1 - 2 during normal operation. The solder points connects the DSP to the JTAG interface port.

### 5.2.3 Interfaces

| Signal | I/O | Description |
|---|---|---|
| JTMS | I | JTAG interface control signal |
| JTCK | I | JTAG interface clock signal |
| JTDI | I | JTAG interface data input signal |
| 25 MHZ | O | Clock output for the B-channel control circuit |
| DSPRDY | I | Interrupt from the data exchange port |
| STINT | I | Interrupt from the status port |
| CHINT | I | Interrupt from the B-channel ontrol circuit |
| MINT | I | Interrupt from the Layer II port |
| STFLAG | I | Not used in current design |

*Table 5.4 Input/Output Lines, Signal Processing Circuit*

| Signal | I/O | Description |
|---|---|---|
| CONRDY | I | Flags that the triple basic rate interface is ready to receive a data byte via the data exchange port |
| DFCON | I | Flags that a data byte is ready to be read from the triple basic rate interface via the data exchange port |
| PUPRES | I | Reset signal from the status port |
| DSEL | O | Data memory select signal for the data exchange port |
| DMS2 | O | Data memory select signal to the B-channel control circuit |
| DMD8;39 | I/O | 32 bit parallel data memory bus to all data ports |
| DMA0;14 | O | 15 bit parallel data memory address bus to the B-channel control circuit |
| DMWR | O | Data memory write strobe to all B-channel data ports |
| DMRD | O | Data memory read strobe to all B-channel data ports |
| STAT1 | O | Read strobe to the status port |
| CLKSEL | O | Write strobe to the clock selector circuit |
| MDATA_RD | O | Read strobe to the Layer II port |
| MDATA_WR | O | Write strobe to the Layer II port |

*Table 5.4 Input/Output Lines, Signal Processing Circuit (Continued)*

### 5.2.4 Circuit Description

Fig. 5.2 shows a schematic block diagram of the signal processing circuit. The circuit consists of an AD21020 floating point processor equipped with 32kx48 program memory and 32kx32 data memory. The CPU clock is generated by a 25 MHz crystal oscillator.

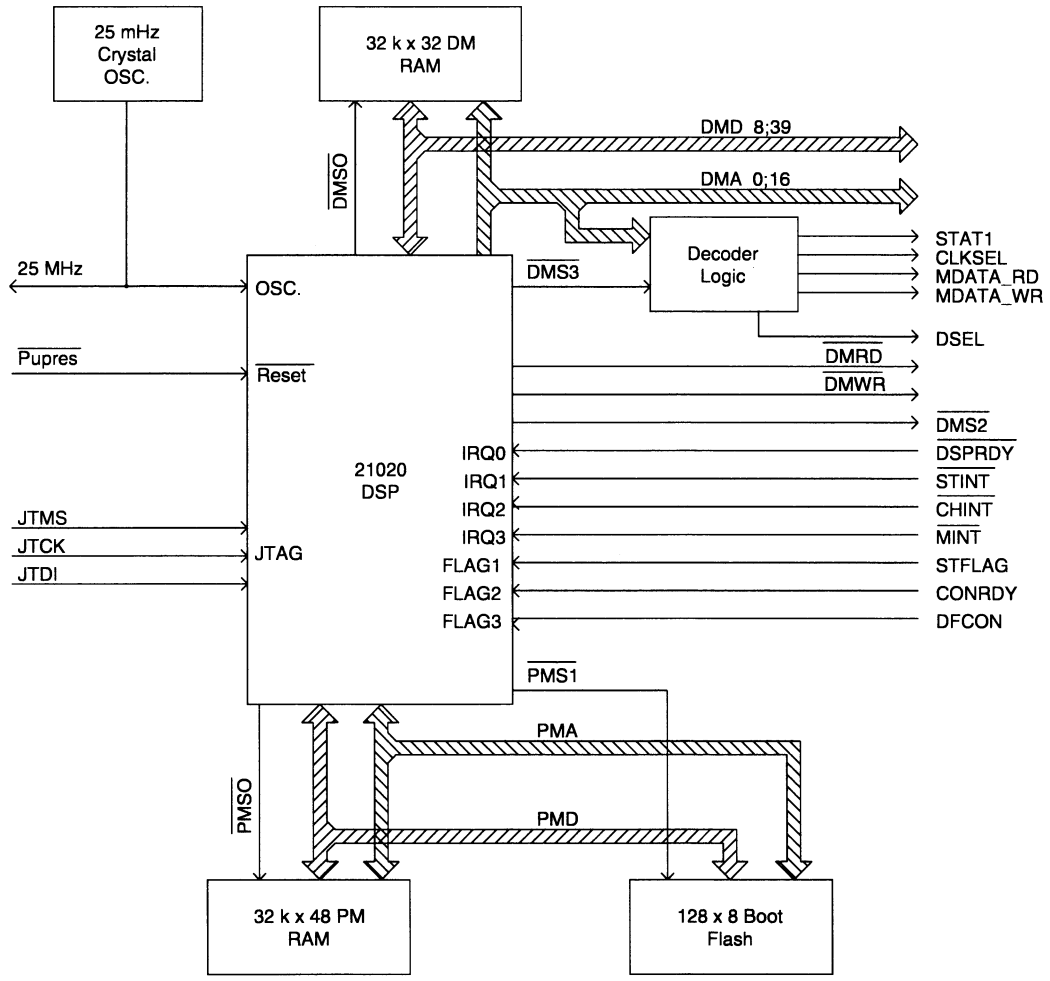


*Fig. 5.2 The Signal Processing Circuit*

After power-up, the triple basic rate interface boots the DSP with a small loader program through the JTAG port. Data to the DSP (JTDI) is clocked in on rising edges of the JTCLK signal. When the loader starts running in the DSP, it loads the splitter/combiner program from the flash prom into the program memory RAM.

After having booted the DSP, the triple basic rate interface signals the initial status of the ISDN B-channels via the status port. This causes the DSP to be interrupted by STINT, it reads the status, sets the frequency of the Layer II clock, and configures the data flow through the DSP accordingly.

The frequency of the Layer II clock is determined by the number of enabled ISDN B-channels and the signaled rate of B-channels A and B.

The signal flow in and out of the DSP is interrupt-controlled by MINT and CHINT. MINT requests 16 bits for output to the Layer II decoder, and another 16 bits are ready as input from the Layer II encoder. CHINT causes the DSP to read the B-channel control circuit to identify which of the six B-channel data ports has caused the interrupt. After that 16 new bits are read from the port as input from the B-channel, and 16 new bits are output to be transmitted via the B-channel. Having serviced the B-channel data port, the DSP clears the interrupt from the B-channel port by writing to the B-channel control circuit.

Data received from the Layer II data port (controlled by MINT) is sequentially split, frame by frame, into data signals for each enabled ISDN B-channel. The splitting sequence of the frames is always in alphabetic order, so that the first frame in each sequence is transmitted via the lowest enabled B-channel (B-channel A when enabled). The private bit in the Layer II header is toggled to define a multi-frame format on each B-channel to allow the combine function in the remote unit to measure and equalize possible transmission delay inequalities between the ISDN B-channels.

The combine function receives its data input from the enabled B-channels. The combiner synchronizes to the Layer II headers on each B-channel and decodes the private bit sequence. By comparing the private bit sequences, the delay inequalities are measured and equalized by delaying the data from the B-channels to an overall equal delay.

The sequence numbers from the status port are then used to determine the sequence to be used to sequentially multiplex the frames from the B-channels into a single serial Layer II signal.

Each B-channel has a sequence number between one and six. A sequence number one indicates that the B-channel conveys the first Layer II frame in each sequence, followed by the channel with sequence number two, and so on.

| | **MSB** | | **Data Bus** | | **LSB** |
|---|---|---|---|---|---|
| **Address** | **39 32** | **31 24** | **23 16** | **15 8** | **7 0** |
| 0000-7FFF | 23k RAM (DMS0) | 23k RAM (DMS0) | 23k RAM (DMS0) | 23k RAM (DMS0) | NA |
| 8000-80FF | NA | NA | NA | NA | NA |
| 8100-81FF | NA | NA | B-ch. A (DMS2) | B-ch. A (DMS2) | NA |
| 8200-83FF | NA | NA | B-ch. B (DMS2) | B-ch. B (DMS2) | NA |

*Table 5.5 Data Memory Map, Signal Processor*

| | MSB | | Data Bus | | LSB |
|---|---|---|---|---|---|
| **Address** | **39 32** | **31 24** | **23 16** | **15 8** | **7 0** |
| 8400-85FF | NA | NA | B-ch. C (DMS2) | B-ch. C (DMS2) | NA |
| 8600-87FF | NA | NA | B-ch. D (DMS2) | B-ch. D (DMS2) | NA |
| 8800-89FF | NA | NA | B-ch. E (DMS2) | B-ch. E (DMS2) | NA |
| 8A00-8BFF | NA | NA | B-ch. F (DMS2) | B-ch. F (DMS2) | NA |
| 8C00-8DFF | NA | NA | NA | NA | NA |
| 8E00-8FFF | NA | NA | B-ch Control (DMS2) | B-ch Control (DMS2) | NA |
| 9000-91FF | Status (DMS3) | Status (DMS3) | Status (DMS3) | Status (DMS3) | NA |
| 9200-93FF | NA | NA | NA | Data Exchg. (DMS3) | NA |
| 9400-95FF | NA | NA | CLK Contr. (DMS3) | CLK Contr. (DMS3) | NA |
| 9600-97FF | NA | NA | Layer II (DMS3) | Layer II (DMS3) | NA |
| 9800- | NA | NA | NA | NA | NA |

*Table 5.5 Data Memory Map, Signal Processor (Continued)*

## 5.3 B-Channel Ports

### 5.3.1 General Description

Each of the six B-channels are interfaced to the signal processing circuit via separate, identical data ports. Each data port is bi-directional and processes 16 bits at a time. The ports are controlled by the B-channel control circuit.

As the six ports designated A, B, C, D, E and F are identical with respect to design, the following sections in this manual are based on the B-channel A port.

### 5.3.2 Interfaces

| Signal | I/O | Description |
|---|---|---|
| TXA | O | Data to be transmitted via ISDN B-channel A |
| RXA | I | Data received from ISDN B-channel A |
| CLKA | I | Bit clock from ISDN B-channel A |
| DMD8;39 | I/O | Data bus from the signal processing circuit |
| ADATA_WR | I | Write strobe from the B-channel control circuit |
| ADATA_RD | I | Read strobe from the B-channel control circuit |
| AINT | O | Interrupt to the B-channel control circuit |

*Table 5.6 Input/Output Lines, B-channel Ports*

### 5.3.3 Circuit Description

Fig. 5.3 shows a schematic block diagram of the B-channel A data port

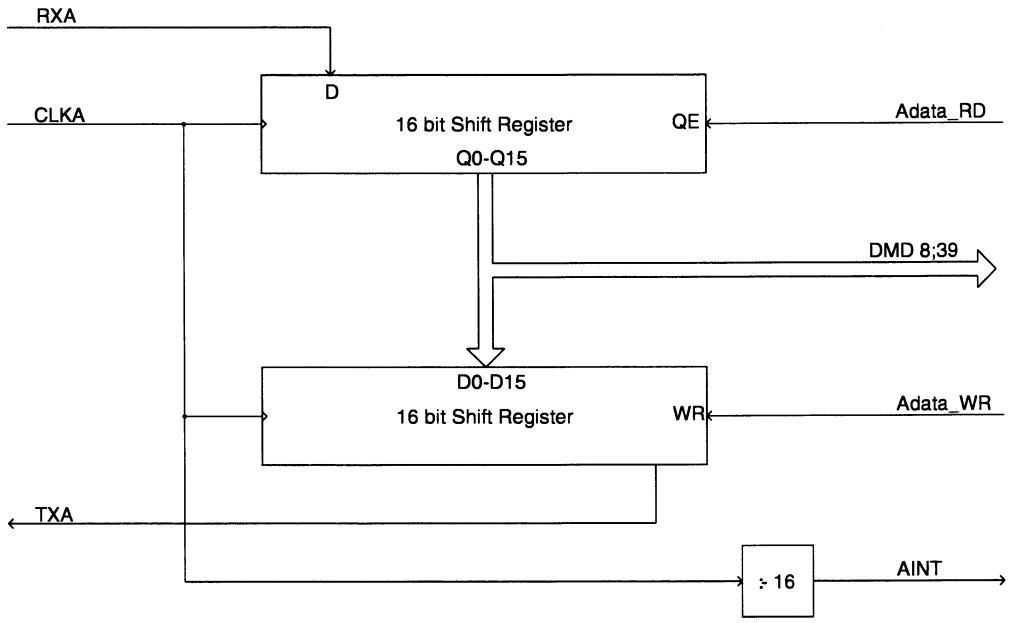


*Fig. 5.3 The B-channel A Data Port*

The circuit comprises a 16-bit serial-to-parallel shift register to input data from the ISDN B-channel to the signal processing circuit, and a 16 bits parallel-to-serial shift register to output data to the B-channel.

Data is clocked in and out of the registers by the B-channel clock signal at 64 (56) kHz. A divide-by-16 circuit generates an interrupt for the B-channel control circuit when new data is ready to be output from the port and new data needs to be input for transmission via the ISDN B-channel.

## 5.4 B-channel Control Circuit

### 5.4.1 General Description

The B-channel control circuit monitors the interrupt signals from the six B-channel data ports to give the signal processing circuit a single interrupt when a port needs service.

### 5.4.2 Interfaces

| Signal | I/O | Description |
|---|---|---|
| DMA0;14 | I | 15 bit address bus from the signal processing circuit |
| DMS2 | I | Address selector bit from the signal processing circuit |
| DMWR | I | Write strobe from the signal processing circuit |
| DMRD | I | Read strobe from the signal processing circuit |
| DMD8;39 | I/O | 32 bit data bus from the signal processing circuit |
| 25 MHZ | I | Clock signal from the signal processing circuit |
| CHINT | O | Interrupt to the signal processing circuit |
| AINT | I | Interrupt from the B-channel A data port |
| BINT | I | Interrupt from the B-channel B data port |
| CINT | I | Interrupt from the B-channel C data port |
| DINT | I | Interrupt from the B-channel D data port |
| EINT | I | Interrupt from the B-channel E data port |
| FINT | I | Interrupt from the B-channel F data port |
| ADATA_WR | O | Write strobe to the B-channel A data port |

*Table 5.7 Input/Output Lines, B-channel Control Circuit*

| Signal | I/O | Description |
|---|---|---|
| ADATA_RD | O | Read strobe to the B-channel A data port |
| ADATA_WR | O | Write strobe to the B-channel B data port |
| ADATA_RD | O | Read strobe to the B-channel B data port |
| ADATA_WR | O | Write strobe to the B-channel C data port |
| ADATA_RD | O | Read strobe to the B-channel C data port |
| ADATA_WR | O | Write strobe to the B-channel D data port |
| ADATA_RD | O | Read strobe to the B-channel D data port |
| ADATA_WR | O | Write strobe to the B-channel E data port |
| ADATA_RD | O | Read strobe to the B-channel E data port |
| ADATA_WR | O | Write strobe to the B-channel F data port |
| ADATA_RD | O | Read strobe to the B-channel F data port |

*Table 5.7 Input/Output Lines, B-channel Control Circuit (Continued)*

### 5.4.3 Circuit Description

Fig. 5.4 shows a schematic block diagram of the B-channel control circuit.

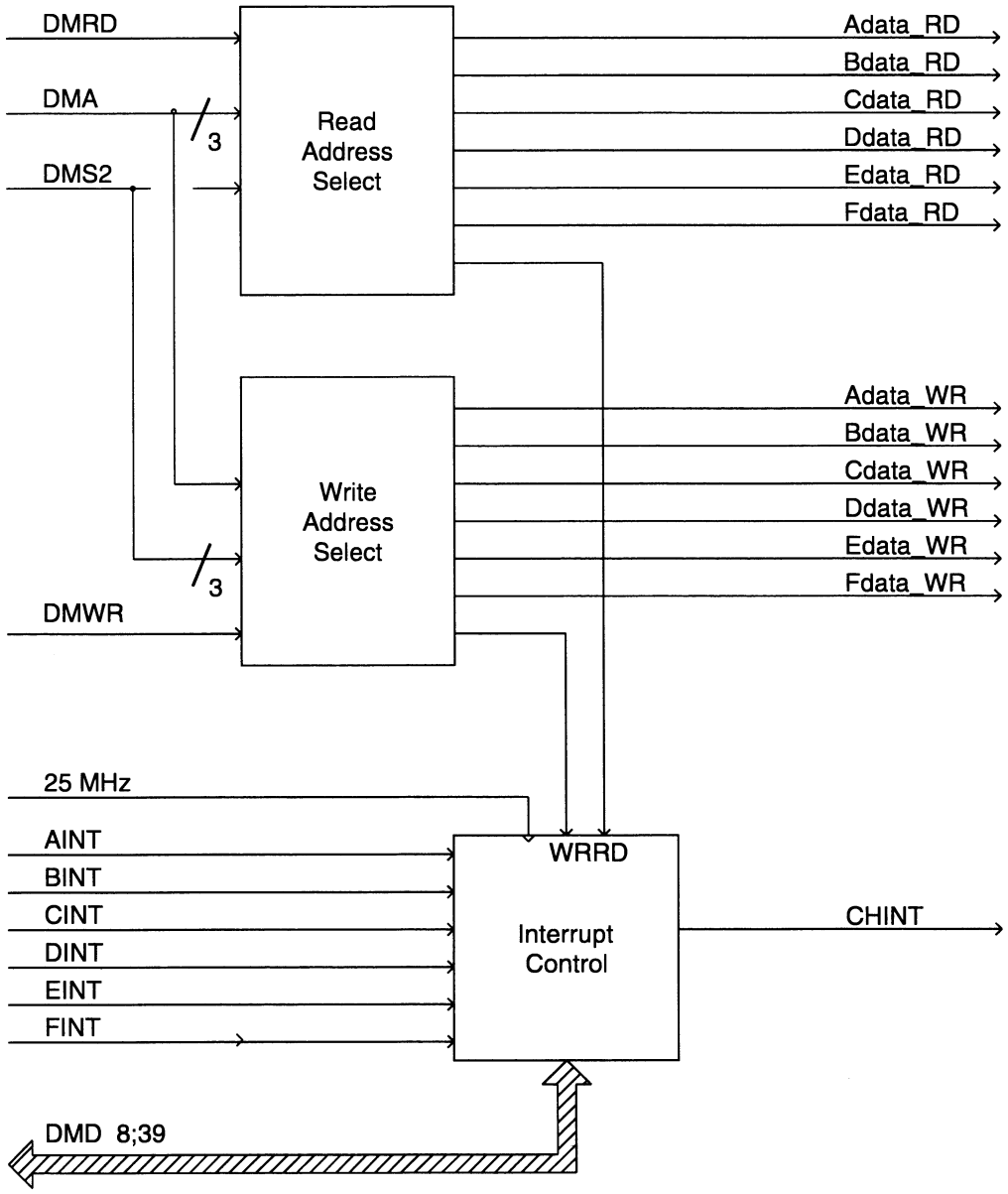


*Fig. 5.4 The B-channel Equalizer Control Circuit*

When a B-channel needs service by the signal processing circuit, the interrupt controller receives a rising edge on AINT, BINT, CINT, DINT, EINT, or FINT, depending on the B-channel in question. The interrupt controller interrupts the signal processing circuit by a low level on CHINT. The signal processing unit reads the interrupt control circuit to

identify the B-channel data port causing the interrupt. Then the signal processing circuit reads from and writes to the port and clears the B-channel's interrupt in the interrupt control circuit.

## 5.5 Clock Control Circuit

### 5.5.1 General Description

The clock control circuit is a programmable clock generator used to generate the Layer II bit clock locked to the rate of ISDN.

### 5.5.2 Interfaces

| Signal | I/O | Description |
|---|---|---|
| CLKA | I | Bit clock from ISDN B-channel A (So1) |
| CLKB | I | Bit clock from ISDN B-channel B (So1) |
| CLKC/D | I | Bit clock from ISDN B-channel C and D (So2) |
| CLKE/F | I | Bit clock from ISDN B-channel E and F (So3) |
| CLKSEL | I | Write strobe from the signal processing circuit |
| DMD8;39 | I | 32 bits data bus from the signal processing circuit |
| MCLK | O | Clock to the Layer II data port |

*Table 5.8 Input/Output Lines, Clock Control Circuit*

### 5.5.3 Circuit Description

Fig. 5.5 shows a schematic block diagram of the clock control circuit.

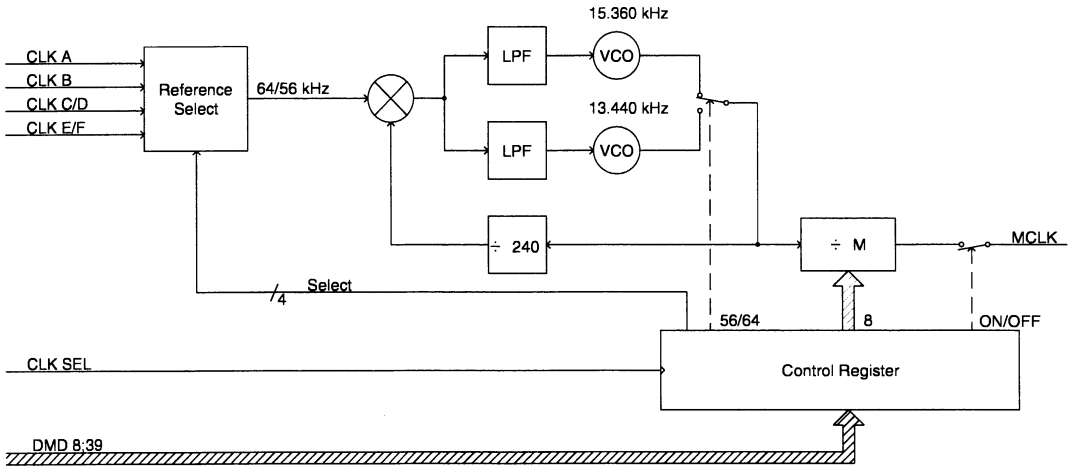


*Fig. 5.5 The Clock Control Circuit*

CLKA, CLKB, CLKC/D, and CLKE/F is input to a reference selector, where one of the clock signals, depending on which B-channel(s) is enabled, is selected as reference input to generate the Layer II clock. The B-channel clock frequency is always 64 kHz, except when B-channel A or B communicates with a switched 56 kbit/s terminal. When the reference is 64 kHz, it is used to lock a 15.360 kHz oscillator, or when it is 56 kHz the 13.440 kHz oscillator is locked to the selected reference. The oscillator output is divided by M to produce the Layer II clock. The divider M is dependent on the number of enabled B-channels as shown in Table 5.9.

| Number of enabled B-channels | Clock frequency |
|---|---|
| 0 | 0 |
| 1 | 64 kHz (or 56 kHz) |
| 2 | 128 kHz (or 112 kHz) |
| 3 | 192 kHz |
| 4 | 256 kHz |
| 5 | 320 kHz |
| 6 | 384 kHz |

*Table 5.9 Layer II Clock Frequencies*

All selections are made by the signal processing circuit based on input from the status port. The signal processing circuit has a 16-bit control register, to which selections are written. The format of the control register is shown in Table 5.10.

| Bit Position | Function |
|---|---|
| DMD8 | Enables the Layer II clock output, when low |
| DMD9 | Selects CLKA as reference, when low |
| DMD10 | Selects CLKB as reference, when low |
| DMD11 | Selects CLKC/D as reference, when low |
| DMD12 | Selects CLKE/F as reference, when low |
| DMD13 | Unused |
| DMD14 | Unused |
| DMD15 | Selects the 15.360 kHz VCO when low; otherwise the 13.440 kHz VCO is selected |
| DMD16 | Divider control LSB |
| DMD17 | Divider control |
| DMD18 | Divider control |
| DMD19 | Divider control |
| DMD20 | Divider control |
| DMD21 | Divider control |
| DMD22 | Divider control |
| DMD23 | Divider control MSB |

*Table 5.10 Format of the Control Register*

### 5.5.4 Adjustments

A diagram showing the location of the adjustable components on the B-channel equalizer is shown in Chapter 5.9. For the clock control circuit, the following adjustments can be made:

The adjustments require the use of a +8 V DC source and a frequency counter.

### 15.360 kHz VCO Adjustment

1. Short-circuit TP2.
2. Inject +8 V DC +/- 0.1 V across R31 with the ground terminal toward TP2.
3. Connect the frequency counter to QD79, pin 6.
4. Tune L4 until the frequency counter reads 15.360 kHz +/- 100ppm.

### 13.440 kHz VCO Adjustment

1. Short-circuit TP1.
2. Inject +8 V DC +/- 0.1 V across R18 with the ground terminal toward TP1.
3. Connect the frequency counter to QD79 pin 3.
4. Tune L4 until the frequency counter reads 13.440 kHz +/- 100ppm.

## 5.6 Layer II Port

### 5.6.1 General Description

The Layer II data port is used to output the restored serial Layer II data signal to the Layer II decoder, and to input Layer II data from the Layer II encoder board to be transmitted via the ISDN B-channels.

### 5.6.2 Interfaces

| Signal | I/O | Description |
|---|---|---|
| Signal | I/O | Description |
| TXDATA | I | Layer II data from the Layer II encoder board |
| MRXDATA | O | Layer II data received from the Layer II decoder board |
| MCLK | I | Layer II bit clock from the clock control circuit |
| DMD8;39 | I/O | Data bus from the signal processing circuit |
| MDATA_WR | I | Write strobe from the signal processing circuit |
| MDATA_RD | I | Read strobe from the signal processing circuit |
| MINT | O | Interrupt to the signal processing circuit |

*Table 5.11 Input/Output Lines, Layer II Port*

### 5.6.3 Circuit Description

Fig. 5.6 shows a schematic block diagram of the Layer II data port.

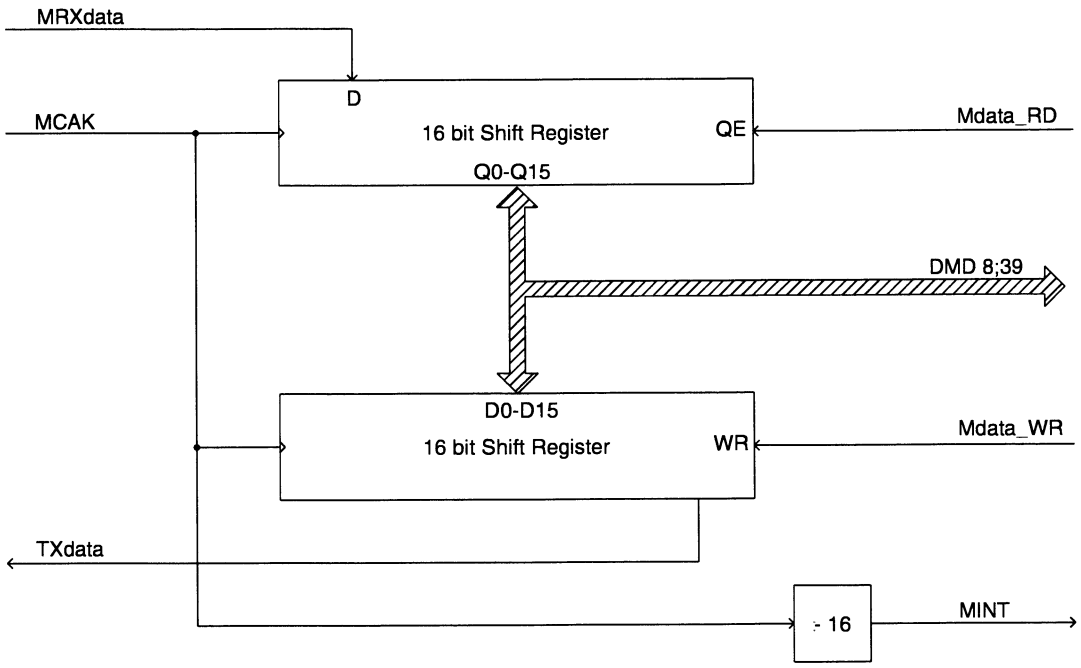


*Fig. 5.6 The Layer II Data Port*

The circuit comprises a 16-bit serial-to-parallel shift register to input data from the Layer II encoder to the signal processing circuit and a 16-bit parallel-to-serial shift register to output data to the Layer II decoder.

Data is clocked in and out of the registers by the Layer II clock signal from the clock control circuit at a rate equal to the capacity of the enabled ISDN B-channels. A divide-by-16 circuit generates an interrupt for the signal processing circuit, when new data is ready to be output from the port and new data needs to be input.

## 5.7 Data Exchange Ports

### 5.7.1 General Description

The data exchange port is a bi-directional, 8-bit parallel port between the signal processing circuit and the triple basic rate interface.

The signal processing circuit uses the port to signal error conditions to the triple basic rate interface, which ports it to download data to the signal processing circuit during software updates.

### 5.7.2 Interfaces

| Signal | I/O | Description |
|---|---|---|
| CS2 | I | Address select signal from the triple basic rate interface |
| A0;7 | I | Address bus from the triple basic rate interface |
| IOWR | I | Write strobe from the triple basic rate interface |
| IORD | I | Read strobe from the triple basic rate interface |
| DSPRDY | O | Hand shake signal to the triple basic rate interface and to the signal processing circuit |
| DFDSP | O | Hand shake signal to the triple basic rate interface |
| D0;7 | I/O | Data bus from the triple basic rate interface |
| DSEL | I | Address select signal from the signal processing circuit |
| DMWR | I | Write strobe from the signal processing circuit |
| DMRD | I | Read strobe from the signal processing circuit |
| CONRDY | O | Hand shake signal to the signal processing circuit |
| DFCON | O | Unused in current design |
| DMD8;39 | I/O | Data bus from the signal processing circuit |

*Table 5.12 Input/Output Lines, Data Exchange Ports*

### 5.7.3 Circuit Description

Fig. 5.7 shows a schematic block diagram of the data exchange port.

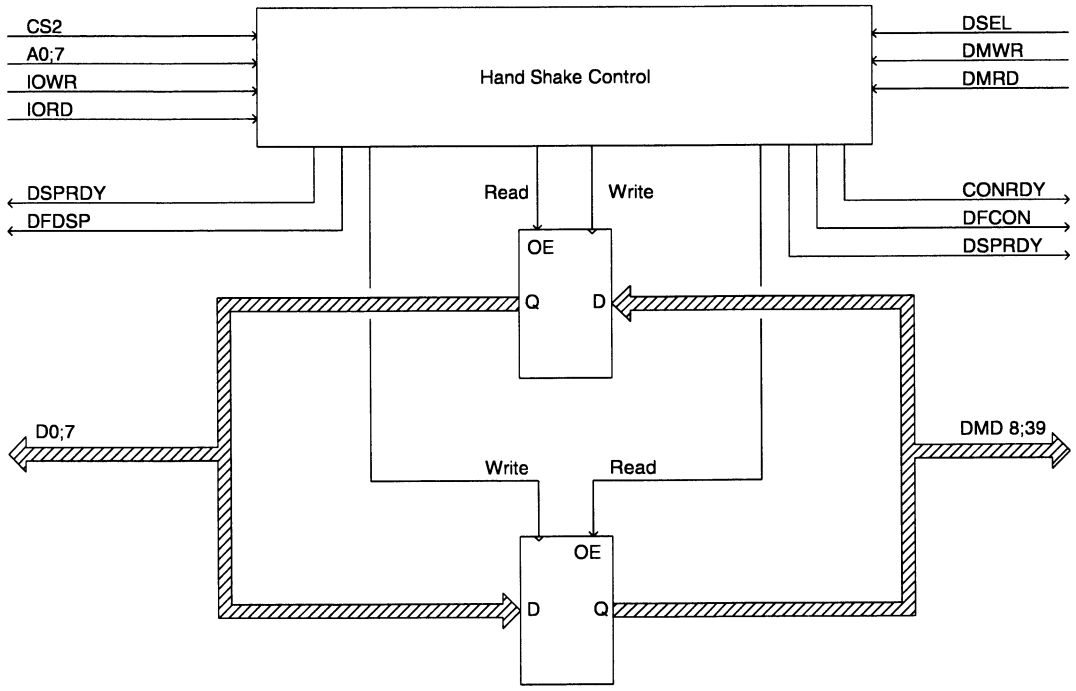


*Fig. 5.7 The Data Exchange Port*

The direction from the triple basic rate board to the signal processing circuit is only used for software updating the B-channel equalizer board.

The triple basic rate interface write operation to the port de-asserts DSPRDY, which interrupts the signal processing circuit. The signal processing circuit reads the data exchange port and asserts DSPRDY, signaling that the data exchange port is ready for the next data byte.

The direction from the signal processing circuit to the triple basic rate interface is used to signal fault conditions and as a control path during software updates.

When a data byte is ready to be read by the triple basic rate interface, DFDSP is asserted. When the triple basic rate interface reads the byte, DFDSP and CONRDY are de-asserted signaling that the data exchange port is ready to receive a new byte from the signal processing circuit.

## 5.8 X.21 Interface

### 5.8.1 General Description

The purpose of the X.21 interface is to allow access to the reverse feed (from the RE 663 ISDN Layer II Decoder to the RE 662 ISDN Layer II Encoder).

The reverse feed can be utilized for bi-directional Layer II transmissions, or it can be utilized for up to two transparent 56/64 kbit/s data channels.

### 5.8.2 Jumper Settings

The type of interface is selected by internal solder points. The setting of these is different in the RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder, as shown below in Table 5.13.

| SP | RE 662 Data | RE 662 Layer II | RE 663 Data | RE 663 Layer II |
|---|---|---|---|---|
| 3 | 1 - 2 | 1 - 2 | Open | 2 - 3 |
| 4 | 1 - 2 | 1 - 2 | 2 - 3 | 1 - 2 |
| 5 | 1 - 2 | 2 - 3 | Open | Open |
| 6 | Open | 2 - 3 | Open | 2 - 3 |
| 7 | 1 - 2 | Open | 1 - 2 | Open |
| 8 | 1 - 2 | 1 - 2 | 2 - 3 | 1 - 2 |
| 13 | 1 - 2 | X | X | X |
| 14 | 2 - 3 | X | 2 - 3 | X |

X = Not applicable

*Table 5.13 Solder Point Settings*

## 5.9 Adjustable Components

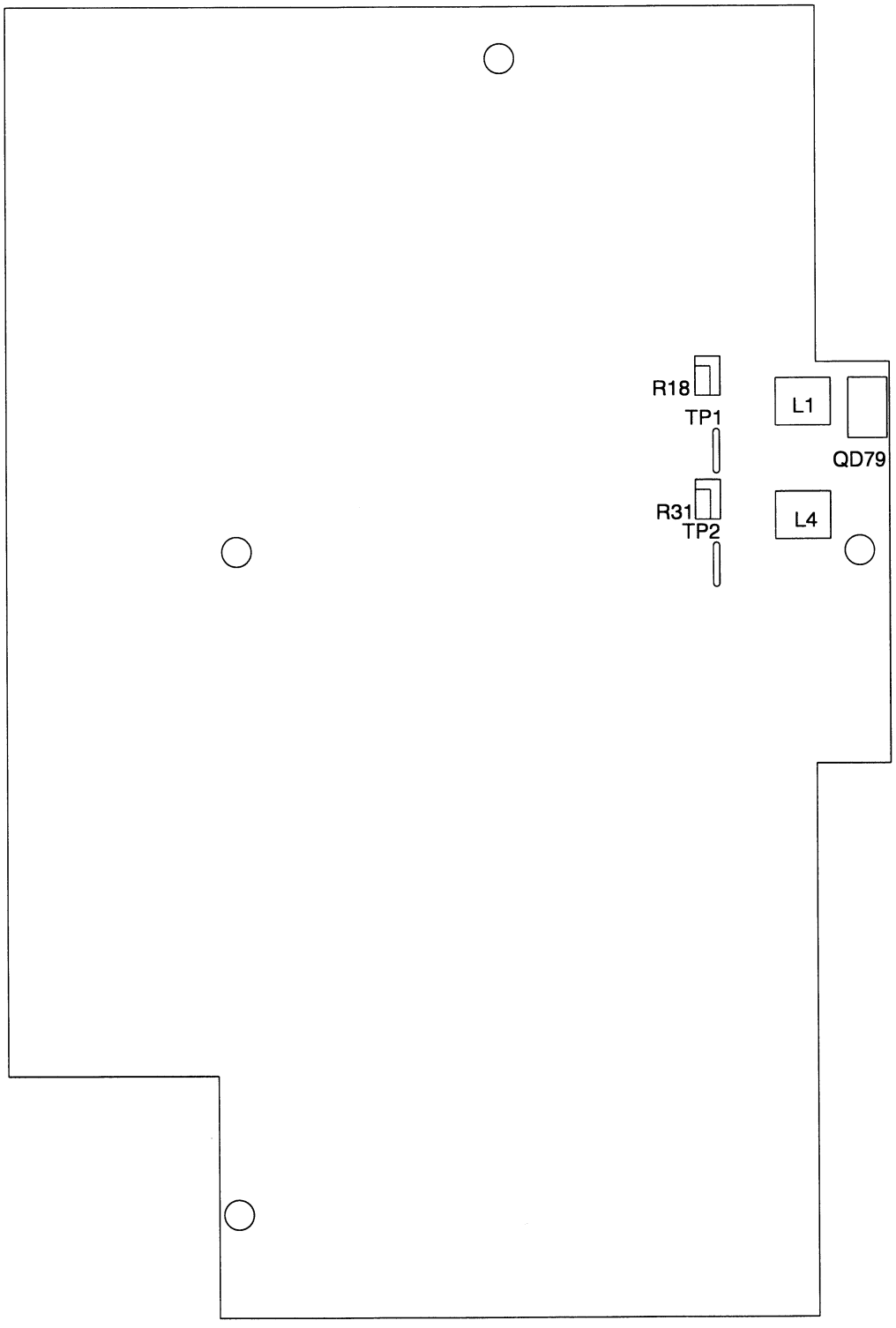


*Fig. 5.8 Adjustable Components on the B-channel Equalizer*

# 6. ISDN Circuits

## 6.1 Introduction

This chapter describes and shows the block diagrams for the triple basic rate interface circuits.

The module has no adjustable components.

## 6.2 So1 Interface

### 6.2.1 General Description

ISDN basic rate So1 interface supports B-channels A and B. The circuit connects directly to ISDN and extracts TX-data, RX-data and a 56 or 64 kHz clock signal from each of the two B-channels. The clock signal is locked to the network, when the B-channel is established.

### 6.2.2 Interfaces

| Signal | I/O | Description |
|---|---|---|
| L1OUT+ | O | Transmit direction to ISDN |
| L1OUT- | O | Transmit direction to ISDN |
| L1IN+ | I | Receive direction from ISDN |
| L1IN- | I | Receive direction from ISDN |
| CLKA | O | Channel A 56/64 kHz clock output to the B-channel equalizer |
| TXA | I | Channel A 56/64 kbit/s data input from the B-channel equalizer |
| RXA | O | Channel A 56/64 kbit/s data output to the B-channel equalizer |
| CLKB | O | Channel B 56/64 kHz clock output to the B-channel equalizer |
| TXB | I | Channel B 56/64 kbit/s data input from the B-channel equalizer |
| RXB | O | Channel B 56/64 kbit/s data output to the B-channel equalizer |
| 12.288 MHZ | O | Master clock to the So2 & So3 interface circuits |

*Table 6.1 Input/Output Lines, So1 Interface*

| Signal | I/O | Description |
|---|---|---|
| A0;23 | I | 3 bit address bus from the controller |
| D0;7 | I/O | 8 bit data bus from the controller |
| IORD | I | Read strobe from the controller |
| IOWR | I | Write strobe from the controller |
| DSCINT1 | O | Interrupt from the DSC to the controller |
| RESDSC1 | I | Reset of the DSC from the controller |
| DSC-CS1 | I | Address select bit to the DSC from the controller |
| ITAINT1 | O | Interrupt from ITAC A to the controller |
| RESITA1 | I | Reset of ITAC A from the controller |
| ITAA-CS1 | I | Address select bit to ITAC A from the controller |
| ITAD-CS1 | I | Address select bit to ITAC A from the controller |
| ITAINT2 | O | Interrupt from ITAC B to the controller |
| RESITA2 | I | Reset of ITAC B from the controller |
| ITAA-CS2 | I | Address select bit to ITAC B from the controller |
| ITAD-CS2 | I | Address select bit to ITAC B from the controller |
| BELL1 | O | Buzzer signal to the voice circuit |
| EAR1_1 | O | Balanced receive voice signal to the voice circuit |
| EAR2_1 | O | Balanced receive voice signal to the voice circuit |
| AIN1 | I | Transmit voice signal from the voice circuit |
| AREF | O | Bias voltage for the AIN1 signal to the voice circuit |

*Table 6.1 Input/Output Lines,* S01 *Interface (Continued)*

### 6.2.3 Circuit Description

Fig. 6.1 shows a schematic block diagram of the S01 Interface.

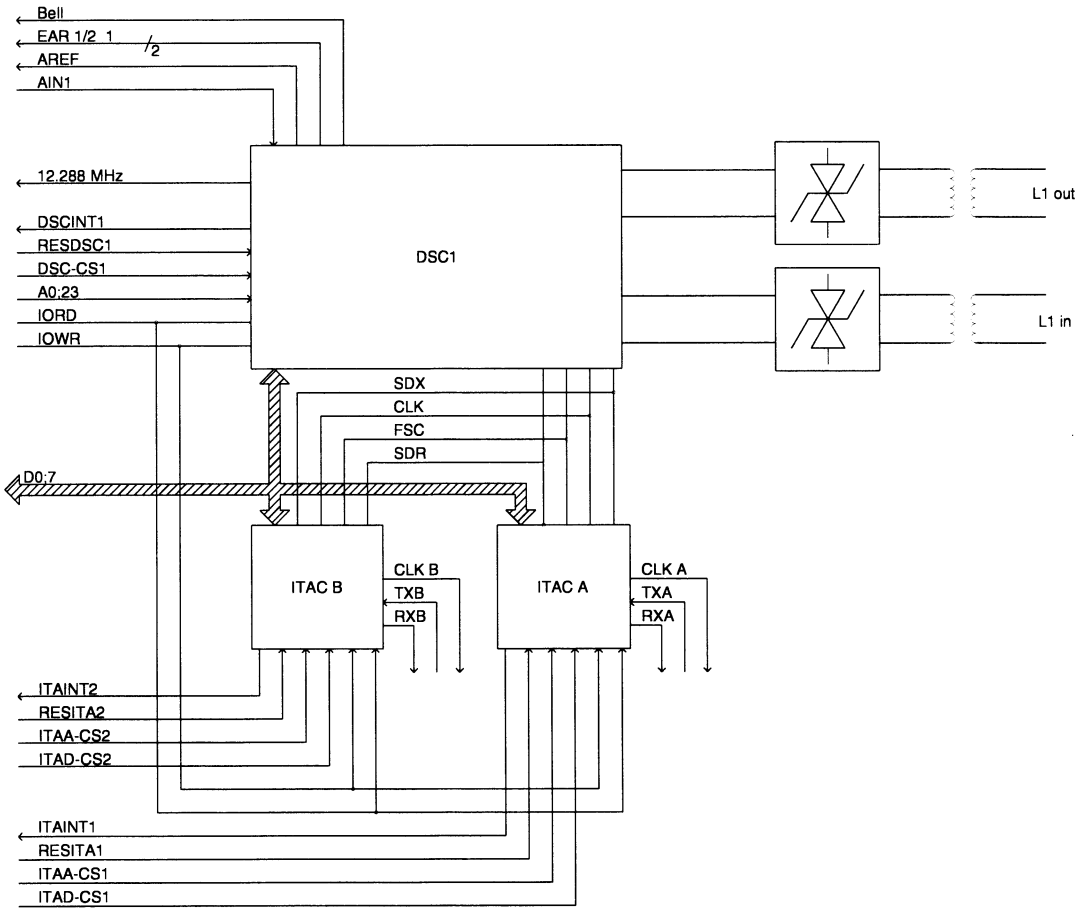


*Fig. 6.1 The S01 Interface*

The line interface of the DSC (Digital Subscriber Controller) connects to the ISDN S-bus interface. It controls time multiplexing and de-multiplexing of the two B-channels, A and B, and the D-channel.

The line interface consists of two parts: a receiver and a transmitter. The receiver section contains a differential receiver and circuitry which recovers bit clock timing, converts the pseudo-ternary coded S-bus signals into binary, and recovers frame synchronization. Collision detection is also performed in order to allow several TEs (Terminal Equipment) to be connected to the same S-bus. The transmitter section converts the binary input into pseudo-ternary pulses which are fed to a differential line driver.

Both the transmit interface and the receive interface are transient-protected and transformer-coupled to give a galvanic separation of the unit from the S-bus.

The D-channel is a 16 kbit/s serial channel which is time-multiplexed within the frame structure on the S-bus. It is used for call setup and call termination. The data is transmitted, encoded, using the Link Access Protocol D channel format, which is defined by ITU for use in ISDN systems.

The triple basic rate interface is capable of receiving and setting up two different types of calls. A voice call, which can be to another ISDN terminal or to a standard analog telephone, or a data call to access an unrestricted 64 kbit/s bearer.

The B-channels are routed to two ITACs (ISDN Terminal Adapter Circuit) via a serial interface when data calls are used. The interface comprises a bit clock signal (CLK), an 8 kHz frame sync (FSC), a transmit (SDX) and a receive data (SDR) signal. The two ITACs each extract their B-channel from the interface to the DSC, and V.110 rate adapt the 64 kbit/s B-channel to 56 kbit/s, when a call has be placed to a switch 56 kbit/s terminal.

The ITACs interface to the B-channel equalizer board by a 56/64 kHz clock (CLKA & CLKB) and a TX (TXA & TXB) and a RX (RXA & RXB) serial data signal which is used to convey the Layer II data.

When performing or receiving a voice call via B-channel A or B, the DSC has an on chip audio codec. This is designed by a digital signal processing architecture with G.711 companding, ADC and DAC featuring a direct signal interface to a hand-set.

Both the DSC and the two ITACs are memory-mapped into the IO-memory of the controller. The controller controls the operation by the So1 interface by various select signals, an address bus and an 8-bit data bus.

## 6.3 So2 and So3 Interface

### 6.3.1 General Description

ISDN basic rate So2 interface supports B-channels C and D, and interface So3 supports B-channels E and F. The circuits, which are identically designed, connect directly to ISDN and extract TX-data, RX-data and the 64 kHz clock signal from each of the two B-channels. The clock signal is locked to the network when the B-channel is established.

The function of the two circuits are equal to the function of So1, with the exception of rate adaptation to 56 kbit/s, which is the reason why the circuit does not comprise any ITACs.

### 6.3.2 Interfaces

| Signal | I/O | Description |
|---|---|---|
| L2OUT+ | O | Transmit direction to ISDN via So2 |
| L2OUT- | O | Transmit direction to ISDN via So2 |
| L2IN+ | I | Receive direction from ISDN via So2 |
| L2IN- | I | Receive direction from ISDN via So2 |
| CLKC/D | O | Channel C and D 64 kHz clock output to the B-channel equalizer |
| TXC | I | Channel C 64 kbit/s data input from the B-channel equalizer |
| RXC | O | Channel C 64 kbit/s data output to the B-channel equalizer |
| TXD | I | Channel D 64 kbit/s data input from the B-channel equalizer |
| RXD | O | Channel D 64 kbit/s data output to the B-channel equalizer |
| 12.288 MHZ | O | Master clock from the So1 Interface circuit |
| A0;23 | I | 3 bit address bus from the controller |
| D0;7 | I/O | 8 bit data bus from the controller |
| IORD | I | Read strobe from the controller |
| IOWR | I | Write strobe from the controller |
| CONTROL2 | I/O | 3 control signal comprising DSCINT2, RESDSC2 and DSC-CS2 to the controller |
| L3OUT+ | O | Transmit direction to ISDN via So3 |
| L3OUT- | O | Transmit direction to ISDN via So3 |
| L3IN+ | I | Receive direction from ISDN via So3 |
| L3IN- | I | Receive direction from ISDN via So3 |
| CLKE/F | O | Channel E and F 64 kHz clock output to the B-channel equalizer |
| TXE | I | Channel E 64 kbit/s data input from the B-channel equalizer |
| RXE | O | Channel E 64 kbit/s data output to the B-channel equalizer |
| TXF | I | Channel F 64 kbit/s data input from the B-channel equalizer |
| RXF | O | Channel F 64 kbit/s data output to the B-channel equalizer |

*Table 6.2 Input/Output Lines, So2 and So3 Interface*

| Signal | I/O | Description |
|---|---|---|
| CONTROL2 | I/O | 4 signals comprising BELL2, EAR1_2, EAR2_2 and AIN2 to the voice circuit |
| CONTROL3 | I/O | 3 control signal comprising DSCINT3, RESDSC3 and DSC-CS3 to the controller |
| 25MHZ | I | Master clock to the data restorer circuits from the controller |

*Table 6.2 Input/Output Lines, So2 and So3 Interface (Continued)*

### 6.3.3 Circuit Description

Fig. 6.2 shows a schematic block diagram of the So2 and So3 interface.

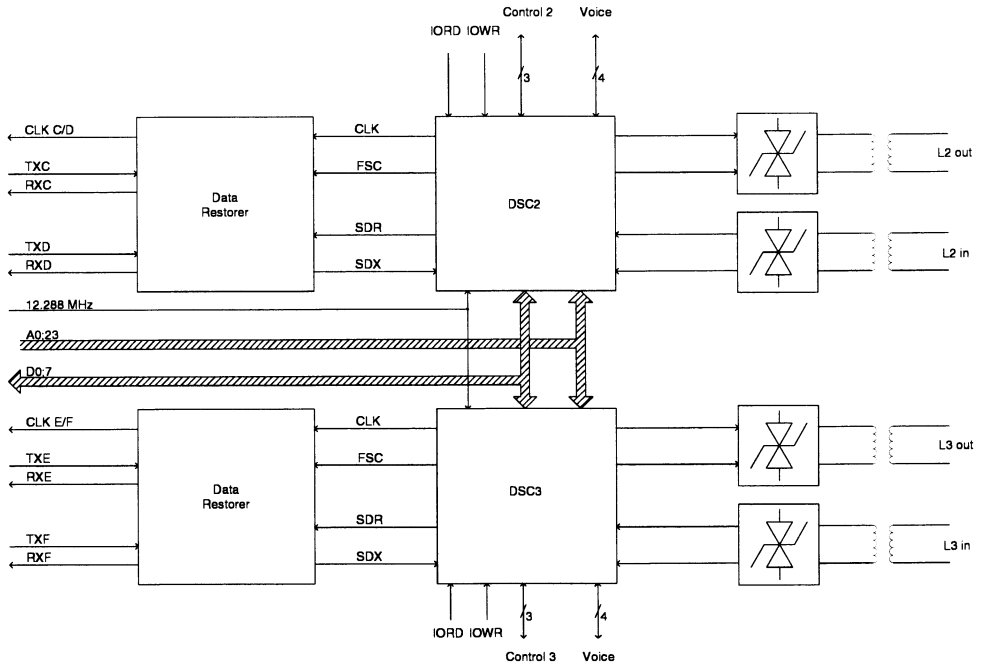


*Fig. 6.2 The So2 and So3 Interface*

As the circuits for the So2 interface and the So3 interface are equal to the So1 interface described above, with the exception of the ITACs, the explanations to the diagram above are limited to the data restorer circuits.

The data extractor circuits are designed by a serial-to-parallel and a parallel-to-serial shift register pair for both the RX and TX direction. Each B-channel is interfaced via a set of shift registers, yielding a total of 8 shift register blocks. The shift registers multiplex and de-multiplex the B-channel data to fit the interface requirements of the DSCs. This process is controlled by a state machine implemented in a PAL.

The state machine generates the required clock signals for the 8 pairs of shift register from the DSC supplied interface signals, CLK and FSC.

## 6.4 Controller

### 6.4.1 General Description

The controller configures and controls the operation of all the circuitry of the triple basic rate interface. The controller is also connected to the B-channel equalizer board, to which the it signals the status on the six ISDN B-channels.

### 6.4.2 Jumper Settings

The circuit includes a number of solder points as shown in Table 6.3. The solder points should always be connected as shown in the table to allow the triple basic rate interface to operate correctly. Different settings of the solder points are reserved for future use.

| Solder Point | Connection |
|---|---|
| SP 1 | 1 - 2 |
| SP 2 | 1 - 2 |
| SP 3 | 1 - 2 |
| SP 4 | 2 - 3 |
| SP 5 | 1 - 2 |
| SP 6 | 1 - 2 |
| SP 7 | OPEN |
| SP 8 | OPEN |
| SP 9 | OPEN |
| SP 10 | OPEN |
| SP 12 | OPEN |
| SP 13 | OPEN |
| SP 14 | 1 - 2 |
| SP 15 | 1 - 2 |
| SP 16 | 1 - 2 |

*Table 6.3 Solder Point Settings in the Controller Circuit*

The controller circuit has a test jumper which can be used to reset both the triple basic rate interface and the B-channel equalizer board. During operation, this jumper shall be open.

| **Jumper** | **JP 1** |
|---|---|
| Reset | 1 - 2 |
| Operation | OPEN |

*Table 6.4 Jumper Settings in the Controller Circuit*

### 6.4.3 Interfaces

| **Signal** | **I/O** | **Description** |
|---|---|---|
| A0;23 | O | 23 bit address bus to other circuitry and to the B-channel equalizer |
| D0;7 | I/O | 8 bit data bus to other circuitry and to the B-channel equalizer |
| IOWR | O | Write strobe to other circuitry and to the B-channel equalizer |
| IORD | O | Read strobe to other circuitry and to the B-channel equalizer |
| 25MHZ | O | Master clock output to the So2 and So3 interfaces |
| RESDSC1 | O | Reset of DSC1 in the So1 interface |
| DSCINT1 | I | Interrupt from DSC1 in the So1 interface |
| DSC-CS1 | O | Chip select of DSC1 in the So1 interface |
| RESDSC2 | O | Reset of DSC2 in the So2 interface |
| DSCINT2 | I | Interrupt from DSC2 in the So2 interface |
| DSC-CS2 | O | Chip select of DSC2 in the So2 interface |
| RESDSC3 | O | Reset of DSC3 in the So3 interface |
| DSCINT3 | I | Interrupt from DSC3 in the So3 interface |
| DSC-CS3 | O | Chip select of DSC3 in the So3 interface |
| RESITA1 | O | Reset of ITAC1 in the So1 interface |
| ITAINT1 | I | Interrupt from ITAC1 in the So1 interface |
| ITAA-CS1 | O | Chip select of ITAC1 in the So1 interface |

*Table 6.5 Input/Output Lines, Controller Circuit*

| Signal | I/O | Description |
|---|---|---|
| ITAD-CS1 | O | Chip select of ITAC1 in the So1 interface |
| RESITA2 | O | Reset of ITAC2 in the So1 interface |
| ITAINT2 | I | Interrupt from ITAC2 in the So1 interface |
| ITAA-CS2 | O | Chip select of ITAC2 in the So1 interface |
| ITAD-CS2 | O | Chip select of ITAC2 in the So1 interface |
| HS_SEL_A | O | Select of allocation of voice channel in the voice circuit, LSB |
| HS_SEL_B | O | Select of allocation of voice channel in the voice circuit, MSB |
| RESET | O | Power-up reset of the B-channel equalizer |
| CS1 | O | Select signal to the B-channel equalizer |
| CS2 | O | Select signal to the B-channel equalizer |
| PUPRES | I | Power-up reset from the Layer II encoder/decoder board |
| I_CTS | I | Handshake signal for communication with the Layer II encoder/decoder board |
| I_RTS | O | Handshake signal for communication with the Layer II encoder/decoder board |
| I_RX | I | Serial data from the Layer II encoder/decoder board |
| I_TX | O | Serial data to the Layer II encoder/decoder board |
| I_FAIL | O | ISDN FAIL alarm signal to Layer II encoder/decoder board |
| R_EM | I | Remote control enabled from the Layer II encoder/decoder board |
| CODE_C0 | I | Remote controlled number group call, LSB from the Layer II encoder/decoder board |
| CODE_C1 | I | Remote controlled number group call from the Layer II encoder/decoder board |
| CODE_C2 | I | Remote controlled number group call, from the Layer II encoder/decoder board |
| CODE_C3 | I | Remote controlled number group call, MSB from the Layer II encoder/decoder board |

*Table 6.5 Input/Output Lines, Controller Circuit (Continued)*

### 6.4.4 Circuit Description

Fig. 6.3 shows a schematic block diagram of the controller circuit.

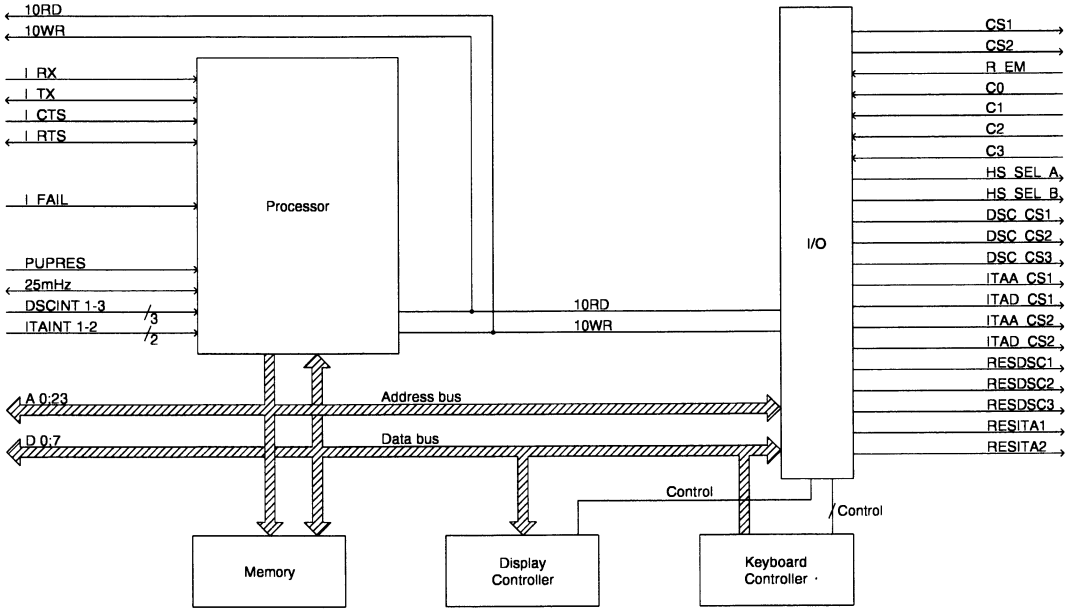


*Fig. 6.3 The ISDN Controller Circuit*

The processor circuit is based on a NEC V53 processor, which is compatible with Intel 8086/8088 architecture but includes additional on-chip peripherals such as timers and an asynchronous serial interface.

The V53 has access to a memory block comprising 2 Mbit of flash PROM, 2 Mbit of RAM for data memory and 64k of E²PROM. The flash prom works as program memory to allow electrical software updates, as does all other circuitry within the RE 662 and RE 663 ISDN Layer II Codec. The E²PROM is used to store telephone numbers and configuration settings.

The keyboard controller is memory mapped into the IO map of the CPU. The keyboard interface is a four-by-four matrix, where the CPU writes all ones to four of the wires. When a key is pressed, one of the four receive wires goes high, interrupting the CPU. The CPU then sequentially pulls each of the four wires low to detect exactly which key has been pressed.

The display is fairly slow, so it has been equipped with a separate controller designed in a PAL. The CPU can freely write to the control circuit, which controls the display by use of a set of handshake signals.

## 6.5 Voice Circuit

### 6.5.1 General Description

The voice circuit comprises a selector block, by means of which the controller can connect the hand-set, the buzzer and front panel LED to the appropriate DSC, dependent on which of the six B-channels is used for the voice call.

### 6.5.2 Interfaces

| Signal | I/O | Description |
|---|---|---|
| HS_SEL_A | I | Access select LSB from the controller |
| HS_SEL_B | I | Access select MSB from the controller |
| BELL1 | I | Buzzer signal from DSC1 |
| BELL2 | I | Buzzer signal from DSC2 |
| BELL3 | I | Buzzer signal from DSC3 |
| AIN1 | O | Voice from hand-set to DSC1 |
| AIN2 | O | Voice from hand-set to DSC2 |
| AIN3 | O | Voice from hand-set to DSC3 |
| EAR1_1 | I | Balanced voice input to hand-set from DSC1 |
| EAR2_1 | I | Balanced voice input to hand-set from DSC1 |
| EAR1_2 | I | Balanced voice input to hand-set from DSC2 |
| EAR2_2 | I | Balanced voice input to hand-set from DSC2 |
| EAR1_3 | I | Balanced voice input to hand-set from DSC3 |
| EAR2_3 | I | Balanced voice input to hand-set from DSC3 |
| AREF | I | Bias voltage from DSC1 |
| VO+ | O | Balanced output to the hand-set |
| VO- | O | Balanced output to the hand-set |
| VI | I | Input from the hand-set |

*Table 6.6 Input/Output Lines, Voice Circuit*

### 6.5.3 Circuit Description

Fig. 6.4 shows a schematic block diagram of the voice circuit.

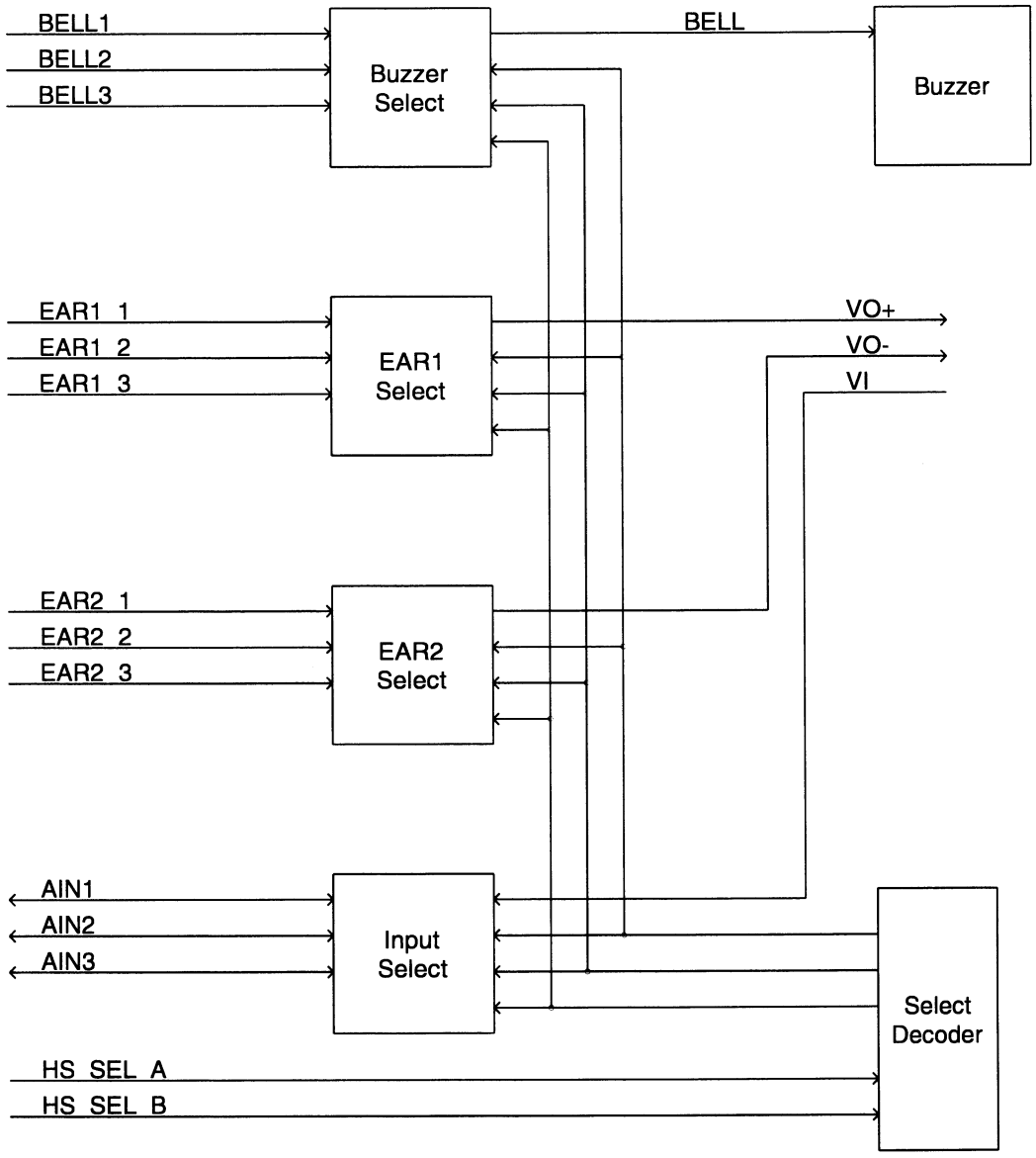


*Fig. 6.4 The Voice Circuit*

The controller generates an enable signal in the select decoder by setting HS_SEL_A and B to either 00, 01 or 10. The enable signal gives the selected DSC access to the buzzer and the front panel hand-set jack.

# 7. Layer II Decoder Circuits

## 7.1 Introduction

This chapter describes and shows the block diagrams for the circuits on the Layer II decoder board.

Fig. 7.11 shows a diagram of the locations of the adjustable components on the decoder board.

## 7.2 Controller

### 7.2.1 General Description

The controller monitors the status of the decoder and controls the Layer II related internal devices according to that status.

Status information is signaled to the front panel display, to the front panel LEDs and to the rear panel alarm/remote connector. Auxiliary data is received from the FIFO and transmitted to the RS-232 interface.

### 7.2.2 Interfaces

The micro controller communicates with the rest of the system through several on-chip I/O bits, externally mapped I/O ports and interrupt lines. Table 7.1 shows a description of the on-chip I/O bits. Table 7.2 shows a description of the decoded I/O selects on the controller block.

| Bit | Name | I/O | Description | Source/Destination |
|---|---|---|---|---|
| P1.0 | /EN_LOW_FLASH | O | "0" indicates FLASH enabled in lower 8k and I/O disabled | |
| P1.1 | /FEMTY | I | "0" indicates FIFO empty | |
| P1.2 | X.21/V35 | O | Not used in this configuration | |
| P1.3 | AESTX_INT | INT | Interrupt from digital/audio transmitter on rising edge | From digital audio input |
| P1.4 | /AESRX_INT | INT | Interrupt from digital/audio receiver on falling edge | From digital audio input |
| P1.5 | RS | O | LCD display register select signal | |
| P1.6 | R/W | O | LCD display Read/Write strobe | |
| P1.7 | E | O | LCD display enable signal | |
| P3.2 | /AUXINT | INT | Interrupt from UART on falling edge | From RS-232 circuit |
| P3.3 | /FRQINT | INT | Interrupt from frequency counter on falling edge | From clock control circuit |
| P4.0 | LCD0 | I/O | LCD display data bus bit 0 | |
| P4.1 | LCD1 | I/O | LCD display data bus bit 1 | |
| P4.2 | LCD2 | I/O | LCD display data bus bit 2 | |
| P4.3 | LCD3 | I/O | LCD display data bus bit 3 | |
| P4.4 | LCD4 | I/O | LCD display data bus bit 4 | |
| P4.5 | LCD5 | I/O | LCD display data bus bit 5 | |
| P4.6 | LCD6 | I/O | LCD display data bus bit 6 | |
| P4.7 | LCD7 | I/O | LCD display data bus bit 7 | |
| P5.0 | INT/EXT | I | Not used in this configuration | |
| P5.1 | NET_FAULT | O | Fail to establish a call or loss of circuit during transmission | From triple basic rate board |
| P5.2 | LCA_DONE | I/O | "1" = LCA active after configuration. If forced low: reprogramming | From clock control circuit |
| P5.3 | LCA_RDY | I | "0" = ready , "1" = busy during configuration load | From clock control circuit |

*Table 7.1 On-Chip I/O Bits, Decoder*

| Bit | Name | I/O | Description | Source/Destination |
|---|---|---|---|---|
| P5.4 | /LCA_INIT | I | "0" indicates LCA in power-up state and not ready | From clock control circuit |
| P5.5 | JTCK | O | Clock bit for JTAG interface | To dec. DSP circuit |
| P5.6 | JTDI | O | Data bit for JTAG interface | To dec. DSP circuit |
| P5.7 | JTMS | O | Mode select for JTAG interface | To dec. DSP circuit |
| P6.3 | EBU-SPDIF | I | Defines the digital audio output format. "1"=SPDIF, "0"=AES/EBU | From digital audio output |
| P6.6 | DFDSP | I | "1" indicates data from DSP | From data exchange port |
| P6.7 | DSPRDY | I | "1" indicates DSP ready, i.e. it has read the last written byte of data | From data exchange port |

*Table 7.1 On-Chip I/O Bits, Decoder (Continued)*

| Signal | Description | Range |
|---|---|---|
| /FIFORD | Read strobe to the FIFO register | 0x00-0x1F |
| /REM1WR | Write strobe to LSB of the remote monitor port | 0x00-0x1F |
| /REM2WR | Write strobe to MSB of the remote monitor port | 0x20-0x3F |
| /STAT1RD | Read strobe to LSB part of status port | 0x20-0x3F |
| /STAT2RD | Read strobe to MSB part of status port | 0x40-0x5F |
| /S8 | Decoded chip select signal to the LCA (QD18) | 0xE0-0xFF |
| /DEXRD | READ strobe to data exchange port | 0xC0-0xDF |
| /DEXWR | Write strobe to data exchange port | 0xC0-0xDF |
| /S5 | Decoded chip select signal to the UART | 0x80-0x9F |
| /AESTXCS | Decoded chip select signal to the digital/audio transmitter | 0x60-0x7F |
| /AESRXCS | Decoded chip select signal to the digital/audio receiver | 0xA0-0xBF |

*Table 7.2 Decoded External I/O Selects, Decoder*

### 7.2.3 Circuit Description

Fig. 7.1 shows a block diagram of the controller circuit.

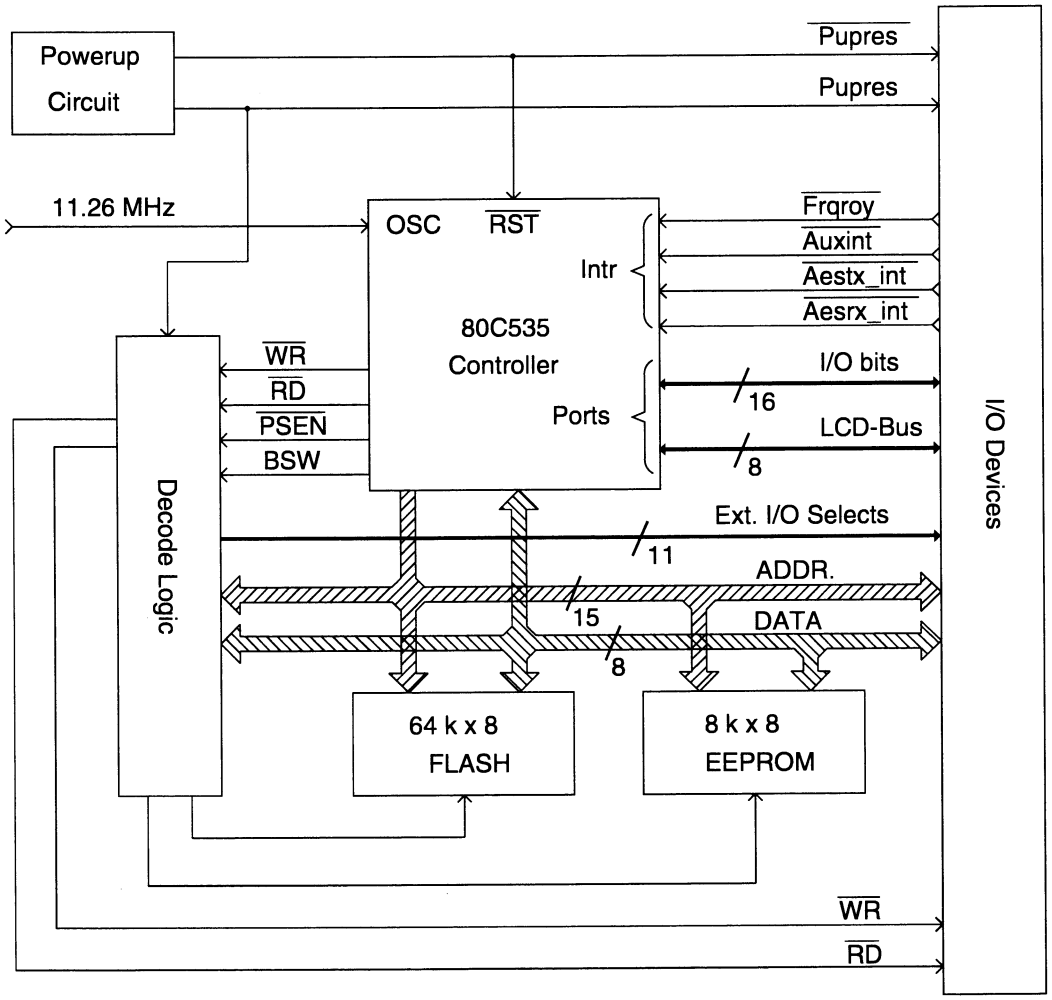


*Fig. 7.1 Layer II Decoder Controller Circuit*

The controller consists of an 80C535 micro controller equipped with 64 kbyte external FLASH memory (QD3) and 8 kbyte external EEPROM memory (QD65). The 8 kbyte of EEPROM memory is bank switched with the top 8 kbyte of FLASH memory. When the bank switch signal (BSW) is high, the EEPROM is selected.

### If EN_LOW_FLASH = "1":

The bottom 8 kbyte of the external memory is mapped as external I/O for data memory transfers and as FLASH memory for program memory transfers. The address decoding of the external data memory ports is handled by QD9. External data memory reads from the FLASH are disabled in the bottom 8k by signal EXMEMDIS (QD6,4) which also serves as write protection by disabling the write strobe in the same area. The FLASH memory is write protected during power-up by QD47, and the bottom 8 kbyte is always write protected by QD12.

### If EN_LOW_FLASH = "0":

The bottom 8 kbyte of external memory is mapped as FLASH memory for data and program memory transfers.

The supervisory circuit (QA2) ensures a proper power-up reset pulse both to the controller and to the rest of the system.

Table 7.3 shows a memory map of the external program/data memory of the controller.

| | /EN_LOW_FLASH = "1" | | | | = "0" | |
|---|---|---|---|---|---|---|
| | **Program Memory** | | **Data Memory** | | **Data Memory** | |
| Address: | BSW="0" | BSW="1" | BSW="0" | BSW="1" | BSW="0" | BSW="1" |
| 0000-0FFF | FLASH | | I/O | | FLASH | |
| 1000-1FFF | FLASH | | I/O | | FLASH | |
| 2000-2FFF | FLASH | | | | | |
| 3000-3FFF | - | | | | | |
| 4000-4FFF | - | | | | | |
| 5000-5FFF | - | | | | | |
| 6000-6FFF | - | | | | | |
| 7000-7FFF | - | | | | | |
| 8000-8FFF | - | | | | | |
| 9000-9FFF | - | | | | | |
| A000-AFFF | - | | | | | |
| B000-BFFF | - | | | | | |
| C000-CFFF | - | | | | | |
| D000-DFFF | - | | | | | |
| E000-EFFF | 4k FLASH | E²prom | 4k FLASH | E²prom | 4k FLASH | E²prom |
| F000-FFFF | 4k FLASH | E²prom | 4k FLASH | E²prom | 4k FLASH | E²prom |

*Table 7.3 Controller Memory Map*

## 7.3 RS-232-C Output

### 7.3.1 General Description

The RS-232-C output is used for transmitting received auxiliary data transfers from the Layer II frames. An input channel is available for software updates of the decoder. Possible baud rates are 300, 600, 1200, 2400, 4800 and 9600.

### 7.3.2 Circuit Description

The circuit consists of a SCC2691 UART (QD32) with a 3.6864 MHz crystal for the master clock oscillator. The UART is mapped into the controller's external data memory and selected by the /S5 chip select signal at address 0x80-0x9F.

The controller handles the setup of the UART through eight internal read/write registers selected by A0-A2. When the UART has transmitted a character, it issues an interrupt by asserting the INTR pin. When the interrupt is recognized by the controller, the next character, if any, is written to the UART, and the INTR is deasserted.

QD33 handles level conversion from RS-232 to TTL by means of an internal charge pump using external capacitors C207, C208 to generate ±9 V DC.

The Request To Send signal (RTS) is passively pulled to the ON state by R41 allowing connections to equipment without RTS/CTS handshake. Additionally, signals RI, DCD and DSR are pulled to the ON state by R38, R39 and R40 allowing connections to equipment requiring these signals to be ON.

The physical connection to the RS-232-C channel is made through the 25-pole SUB-D connector (RS-232 OUTPUT) on the rear panel. The decoder is configured as a Data Communications Equipment (DCE) unit.

## 7.4 Alarm and Remote Monitor Circuits

### 7.4.1 General Description

The alarm output located on the rear panel is activated if a fault situation is detected by the controller. Examples of possible faults are ISDN fault, frame loss to the input Layer II signal, or an internal circuit fault.

The remote monitor function allows the decoder to be monitored from a remote location instead of from the front panel.

### 7.4.2 Circuit Description

The alarm circuit is formed by transistor Q7 and the relay K1. The relay is capable of switching up to 50 W. In an alarm situation, the controller switches off Q7, which means that the relay is released, and there is a short-circuit between pins 2 and 15 and an open circuit between pins 1 and 14 in the alarm/remote connector on the rear panel. The alarm circuit is in the alarm position when there is no power to the decoder.

The remote monitor function is implemented using 11 HCMOS output bits with a 100 Ω series resistor for protection. The outputs are always active and reflect the current status of the decoder. The status is the same as displayed in the front panel display. The format of the bits is described in the Operator Manual.

## 7.5 Front Panel

### 7.5.1 General Description

The front panel is controlled by the controller and consists of a 16-character one-line LCD display for displaying status about the setup and three LEDs for displaying information about alarms and status of the decoder.

### 7.5.2 Circuit Description

Communication with the display is made through the LCD data bus (controller P4) with register select (RS), Enable (E) and read/write (R/W) signals controlled from P1 on the controller.

The circuit with Q8 and Q9 supplies the back plane light with a constant current. R123, R124, R58 and R34 determine the contrast of the display.

The three LEDs on the front panel are controlled via an 8-bit external output port (QD1) by the controller. Table 7.4 describes each bit in the LED output port.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| - | - | Frame Loss | Dig. audio lock | ISDN Fault | - | - | - |

*Table 7.4 LED Port Bit Assignment*

## 7.6 Decoder DSP

### 7.6.1 General Description

The decoder DSP handles the decoding of the ISO MPEG Layer II frames. The frames are received from the B-channel equalizer,and the audio information is extracted and decompressed according to the status information read from the header of the frames. After decompression of the audio, it is transmitted to the DAC for analog audio output and to the digital audio transmitter for digital audio output.

When the signaled sample frequency is 16, 22.05 or 24 kHz, the DSP interpolates the audio samples by two to convert the sample frequency to 32, 44.1 or 48 kHz prior to feeding the restored audio samples to the audio output circuits.

### 7.6.2 Circuit Description

The DSP circuit consists of a 21020 floating point processor (QD59) equipped with 32kx48 program memory and 32kx32 data memory. The CPU clock is generated by a 25 MHz Dual In Line (DIL) crystal oscillator (QD60).

After power-up, the controller loads the DSP with a small boot loader program through the JTAG port (J12). Data to the DSP (JTDI) is clocked in on the rising edge of the JTCK signal. The controller starts the DSP, releasing the /DSP_RESET command.

When the loader starts running in the DSP, it loads the decoder program from the 128 kbyte boot FLASH (QD18), which is mapped into program memory space. QD47 ensures write protection of the FLASH during power-up.

Fig. 7.2 shows a block diagram of the decoder DSP.

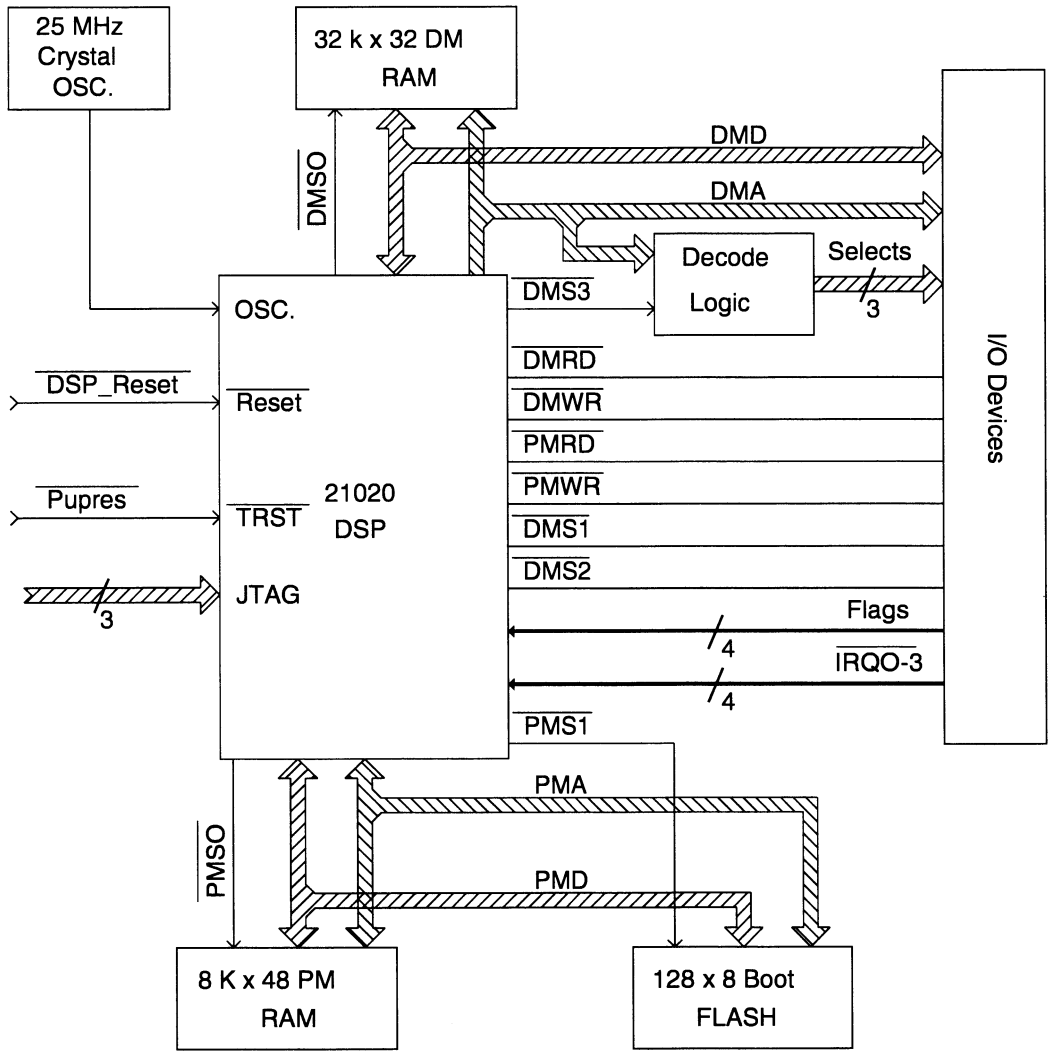


*Fig. 7.2 The Decoder DSP*

The signal flow in and out of the DSP is interrupt controlled using /IRQ1, /IRQ2 and /IRQ3. When data is ready from the B-channel equalizer, the DSP receives an interrupt on /IRQ1. Similarly, data is output to the ADC and digital audio transmitter when requested by an /IRQ3 interrupt from the IIS interface.

QD17 decodes the internally generated select signal /DMS3 into eight sub-decoded select signals. Three of these signals (/DSEL1-DSEL3) are used to select the FIFO register, the data exchange port and the status port.

Table 7.5 shows the data memory map of the decoder DSP.

| Adr. | Decoder Data Memory (DMD Bus) | | | | |
|---|---|---|---|---|---|
| | 39----------32 | 31----------24 | 23----------16 | 15----------8 | 7----------0 |
| 0000h<br>7FFFh | 32k RAM (/DMS0) | | | | FREE |
| 8000h<br>80FFh | IIS write (/DMS1) | | SPI A Read (/DMS1) | | |
| 8100h<br>8FFFh | FREE | | SPI B Read (/DMS2) | | |
| 9000h<br>91FFh | FREE | | | FIFO read (/DSEL1) | |
| 9200h<br>93FFh | FREE | | | DEX rd/wr (/DSEL2) | |
| 9400h<br>95FFh | FREE | | STATUS write (/DSEL3) | | |
| 9600h<br>97FFh | DSEL4 (free) | | | | |
| 9800h<br>9AFFh | DSEL5 (free) | | | | |
| 9A00h<br>9BFFh | DSEL6 (free) | | | | |
| 9C00h<br>9DFFh | DSEL7 (free) | | | | |
| 9E00h<br>9FFFh | DSEL8 (free) | | | | |

*Table 7.5 Decoder DSP Data Memory Map*

## 7.7 IIS Interface

### 7.7.1 General Description

The IIS interface is used to convert the 16-bit parallel data format from the DSP to a 32-bit serial data (IIS) format for the analog and digital audio outputs. Upon interrupt the DSP writes the 16-bit audio samples for left or right channel to the IIS interface.

### 7.7.2 Circuit Description

The parallel data is clocked into the 16-bit parallel-to-serial shift register (QD15, QD18) on the rising edge of the write strobe (QD8,11). When the preceding 16 bits have been output in serial, a parallel load signal (QD13,5) loads the output shift register with the pending 16-bit sample from the input register of QD15 and QD18. After this load, new data can be written to the input registers, and the I²SINT signal goes low to interrupt the DSP.

The DSP is interrupted separately for left and right channel samples, and hence the interrupt frequency is twice the sample frequency. After each interrupt, QD14,6 indicates whether a left or right audio sample is needed.

## 7.8 Serial to Parallel Interface

### 7.8.1 General Description

The serial to parallel interface is used to convert serial data from the B-channel Equalizer into 16-bit parallel words for the DSP. Each channel, A and B, has its own 16-bit converter circuit which interrupts the processor when new data is ready. Please note that channel B circuitry is not used in an RE 663 ISDN Layer II Decoder.

### 7.8.2 Circuit Description

Data from channel A is clocked into registers QD49 and QD50, in serial, on the rising edge of the CLOCK_A signal. After 16 clock periods, QD48 clocks the bits in QD49 and QD50 to their output holding registers, and interrupts the DSP with the interrupt signal /SPIA_INT.

After the DSP is interrupted, it reads the 16-bit data in parallel by enabling the output of the registers QD49 and QD50 through gate QD47,6. When enabled (low level from QD47), the data is present at the DSP databus DMD8-DMD23.

The circuit for channel B operates the same way as channel A, and consists of the registers QD46 and QD63, counter QD48 and gate QD47.

## 7.9 Common DSP and Controller Ports

### 7.9.1 General Description

The controller and the DSP communicate through three ports. A FIFO is used to buffer auxiliary data from the DSP before it is written to the UART. Various information is exchanged between the two processors through a data exchange port (DEX). Additionally, status and setup information is signaled to the controller from the DSP via a status port.

### 7.9.2 FIFO Circuit Description

The FIFO (QD41) is used to buffer auxiliary data from the DSP, so that the controller can read data when requested by the UART. The DSP writes characters to the FIFO in blocks as they are extracted from the MPEG frames. The controller monitors the empty flag (QD41 pin 21). If the empty flag is high, there is data from the DSP, and the controller continues to read the FIFO until the flag goes low. The FIFO internal read/write pointers are reset at power-up by the signal /PUPRES at pin 22.

### 7.9.3 Data Exchange Port Circuit Description

The data exchange port consists of QD42, QD43 and QD44. QD43 and QD44 are used as an 8-bit bi-directional port with input registers and output enable. QD47 serves as a control circuit for the four handshake signals: Data from controller (DFCON), Controller ready (CONRDY), Data from DSP (DFDSP) and DSP ready (DSPRDY).

When the DSP writes data to the controller, the write strobe sets QD42,5 high indicating DFDSP to the controller. Likewise, QD42,9 is set high to indicate DFCON, when the controller writes to the data exchange port. When the receiving processor reads its data, the corresponding bit goes low again and indicates DSPRDY or CONRDY.

### 7.9.4 Status Port Circuit Description

The status port is a 16-bit port formed by QD39, QD45 and QD38. The port is mapped as two 8-bit ports at the controller end and as one 16-bit port at the DSP end.

Status written by the DSP to the LSB part is constantly available to other circuits in the system. The same bits are available to the controller through tristate buffer QD39. The MSB part is only available to the controller.

Tables 7.6 to 7.8 show the status port bits seen from DSP data memory data bus (DMD).

| DMD 23 | DMD 12 | DMD 11 | FS | DMD 10 | MPEG | DMD 9 | DMD 8 | Emphasis |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Reserved | 0 | Unlock | 0 | 0 | None |
| 0 | 0 | 1 | 16.0 kHz | 1 | Lock | 0 | 1 | 50/15 us |
| 0 | 1 | 0 | 22.05 kHz | | | 1 | 0 | Reserved |
| 0 | 1 | 1 | 24.0 kHz | | | 1 | 1 | J.17 |
| 1 | 0 | 0 | Reserved | | | | | |
| 1 | 0 | 1 | 32.0 kHz | | | | | |
| 1 | 1 | 0 | 44.1 kHz | | | | | |
| 1 | 1 | 1 | 48.0 kHz | | | | | |

*Table 7.6 Status Port Bit Definitions*

| DMD15 | DMD14 | DMD13 | Aux. Rate |
|---|---|---|---|
| 0 | 0 | 0 | No aux data |
| 0 | 0 | 1 | 300 baud |
| 0 | 1 | 0 | 600 baud |
| 0 | 1 | 1 | 1200 baud |
| 1 | 0 | 0 | 2400 baud |
| 1 | 0 | 1 | 4800 baud |
| 1 | 1 | 0 | 9600 baud |

*Table 7.7 Status Port Bit Definitions*

| DMD21 | DMD20 | Mode | DMD22 | Transmission |
|---|---|---|---|---|
| 0 | 0 | Stereo | 0 | Redundant |
| 0 | 1 | Joint Stereo | 1 | Split Mode |
| 1 | 0 | Dual Channel | | |
| 1 | 1 | Single Channel | | |

*Table 7.8 Status Port Bit Definitions*

## 7.10 Analog Audio Output

### 7.10.1 General Description

The analog audio output circuit receives three clock signals, one for each of the sample frequencies. The controller signals which sample frequency to use, and the corresponding clock is divided to generate a bit clock and a sample identifier signal used to collect samples from the Layer II decoder.

The samples are converted into a left and right analog signal which are lowpass-filtered, and de-emphasized when signaled by the controller.

The signals are amplified to utilize a maximum output level or -5, -2, +1, +9, +12, +15, +18, +21 or +24 dBu, set by internal jumpers, and buffered by an amplifier with an output impedance of either 600 Ω or <60 Ω.

### 7.10.2 Jumper Settings

The output impedance can be set to 600 Ω or to low impedance (<60 Ω) as shown in Table 7.9. Fig. 7.9 shows the diagram of the location of the adjustable components in the decoder.

| **Output Impedance** | **Left Channel** | | **Right Channel** | |
|---|---|---|---|---|
| **Jumpers** | **TP 1** | **TP 5** | **TP 6** | **TP 7** |
| 600 Ω | 2-3 | 2-3 | 2-3 | 2-3 |
| <60 Ω[a)] | 1-2 | 1-2 | 1-2 | 1-2 |

*Table 7.9 Analog Audio Outputs*

a. Indicates the default setting from RE TECHNOLOGY AS.

The maximum output level can be set to -5, -2, +1, +9, +12, +15, +18, +21 or +24 dBu to meet different requirements for average program levels and head rooms. Note, that a maximum output level of +24 dBu can only be achieved by using the low output impedance option.

| Output Level | SP8 | SP7 | SP9 | SP10 | SP14 | SP13 | SP12 | SP6 |
|---|---|---|---|---|---|---|---|---|
| 24 dBu | 2-3 | 1-2 | 1-2 | 1-2 | 2-3 | 1-2 | 1-2 | 1-2 |
| 21 dBu | 1-2 | 2-3 | 1-2 | 1-2 | 1-2 | 2-3 | 1-2 | 1-2 |
| 18 dBu | 1-2 | 1-2 | 1-2 | 1-2 | 1-2 | 1-2 | 1-2 | 1-2 |
| 15 dBu[a)] | 2-3 | 1-2 | 1-2 | 2-3 | 2-3 | 1-2 | 1-2 | 2-3 |
| 12 dBu | 1-2 | 2-3 | 1-2 | 2-3 | 1-2 | 2-3 | 1-2 | 2-3 |
| 9 dBu | 1-2 | 1-2 | 1-2 | 2-3 | 1-2 | 1-2 | 1-2 | 2-3 |
| 1 dBu | 2-3 | 1-2 | 2-3 | 1-2 | 2-3 | 1-2 | 2-3 | 1-2 |
| -2 dBu | 1-2 | 2-3 | 2-3 | 1-2 | 1-2 | 2-3 | 2-3 | 1-2 |
| -5 dBu | 1-2 | 1-2 | 2-3 | 1-2 | 1-2 | 1-2 | 2-3 | 1-2 |

*Table 7.10 Layer II Decoder Output Level with Output Impedance <60 Ω*

a. Factory setting

**NOTE** If the output impedance is set to 600 Ω, and the output is loaded into 600 Ω, all output levels will be 6 dB lower than stated in Table 7.10.

### 7.10.3 Interfaces

| Signal | Description |
|---|---|
| | Left channel analog audio output to the rear panel |
| | Right channel analog audio output to the rear panel |
| FSEL0 | Sample frequency select (LSB) from the controller |
| FSEL1 | Sample frequency select (MSB) from the controller |
| 8192 kHz | Sample frequency input from the clock control circuit |
| 6144 kHz | Sample frequency input from the clock control circuit (not used in current design) |
| 11289.6 kHz | Sample frequency input from the clock control circuit |
| 12288 kHz | Sample frequency input from the clock control circuit |
| CLK | Bit clock output to the Layer II decoder and digital audio output |
| 256XFS | Master clock signal to the digital audio output |

*Table 7.11 Input/Output Lines, Analog Audio Output*

| Signal | Description |
|---|---|
| WS | Sample identifier output to the Layer II decoder and digital audio output |
| DATA | Serial data input comprising both left and right samples from the Layer II decoder |
| CLK2 | Clock output used to synchronize the data output from the Layer II decoder |
| DACRST | Signal from the controller used to mute and reset the D/A converter during frame loss |

*Table 7.11 Input/Output Lines, Analog Audio Output (Continued)*

### 7.10.4 Circuit Description

Fig. 7.3 shows a block diagram of the analog audio output circuit.

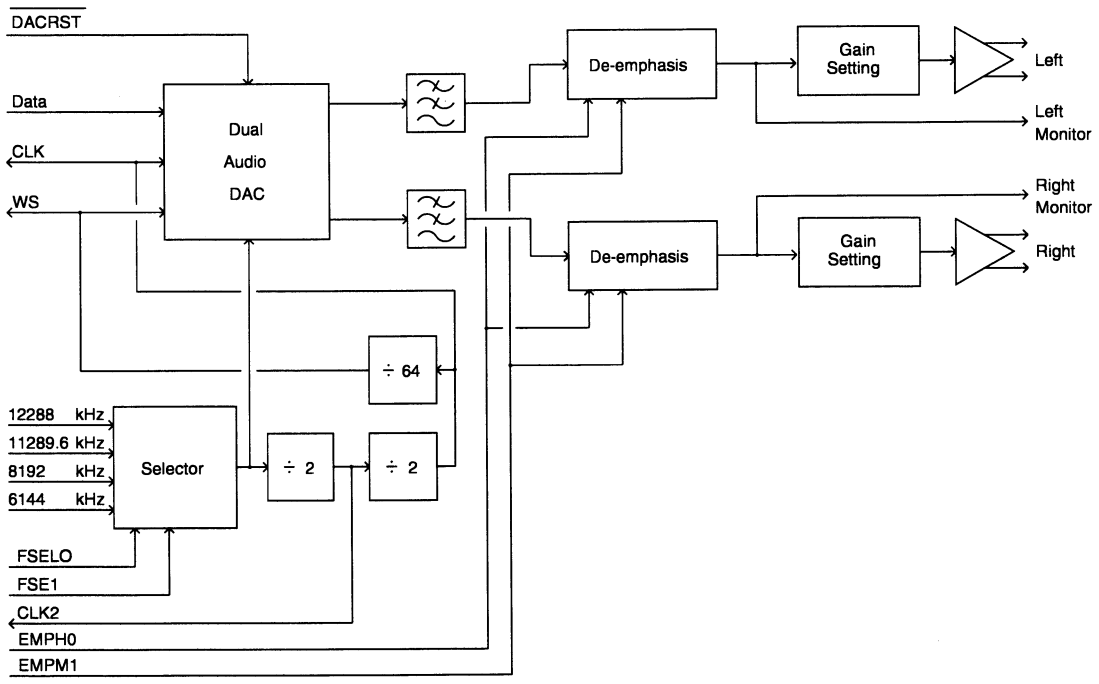


*Fig. 7.3 The Analog Audio Output Circuit*

The analog audio output receives three clock inputs, one for each sample frequency, along with the control signals needed to select the appropriate sample frequency. The selected clock signal is used as the master clock for the DAC, and is divided by two to generate a synchronization frequency used to form samples on the serial data input.

The synchronization signal is divided by two to generate the bit clock used to collect data from the Layer II decoder. Additional division by 64 generates the sample identifier signal which is also used to collect data samples from the Layer II decoder.

The audio samples are converted into the analog domain by the dual DAC. The restored analog signals are lowpass-filtered to remove the high-frequency sampling mirrors and de-emphasized according to the ITU-T J.17 or 50/15 μs specifications when commanded by the controller.

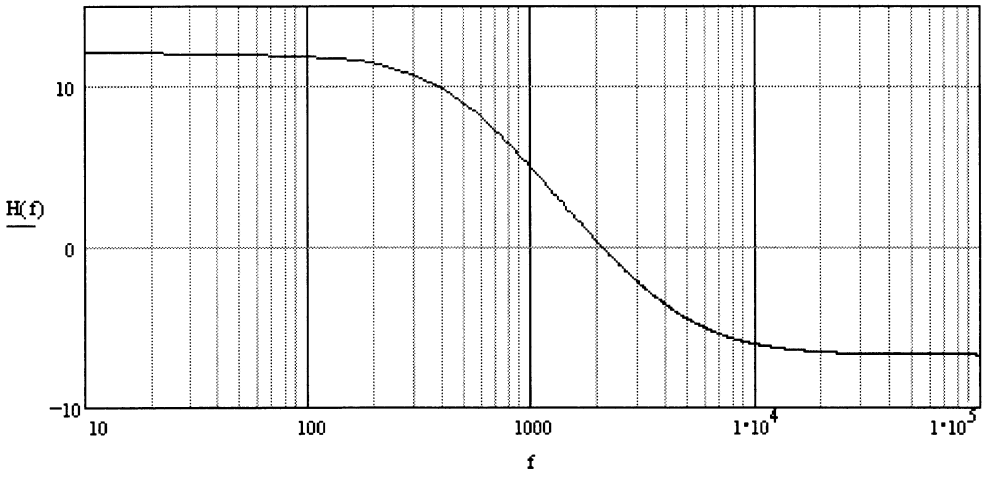


*Fig. 7.4 ITU-T J.17 De-emphasis*

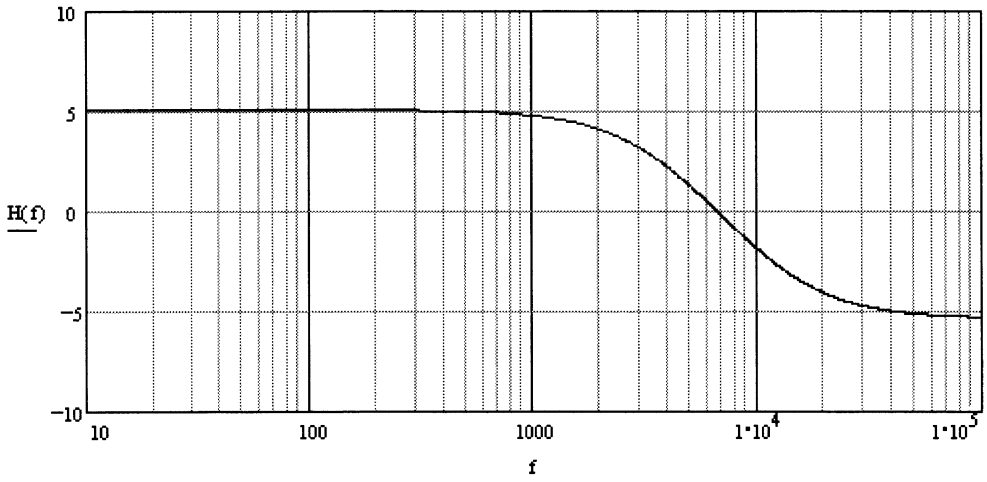


*Fig. 7.5 50/15 μs De-emphasis*

The de-emphasized audio signals are routed to the audio monitor for front panel monitoring and to the analog audio output amplifier circuits. These amplifier circuits are constructed so that their gains are adjustable. The gain can be set by internal jumpers to meet different requirements for average program levels and head rooms. The signals are buffered by an audio output driver which converts the signals to transformer-like balanced signals and passes them to the output connectors with an output impedance of either 600 Ω or <60 Ω.

### 7.10.5 Adjustments

For the analog audio output circuit, only the analog audio gain can be adjusted. Fig. 7.11 shows the location of the adjustable components in the decoder.

The adjustments require the use of:

- A digital audio source (AES/EBU or S/PDIF formats) capable of supplying an output with a digital-generated 1 kHz sine wave with maximum amplitude, that is, all the digital codes are used to represent one cycle.
- A DVM capable of a 1 kHz AC voltage measurements with a resolution and an accuracy better than 0.05 dB.
- A RE 662 ISDN Layer II Encoder.
- Four ISDN basic rate accesses.

#### Left Channel Gain Adjustment

1. Connect the RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder to each their ISDN basic rate access, and establish a minimum of four B-channels.
2. Apply the digital audio signal to the RE 662 ISDN Layer II Encoder.
3. Set the gain and output impedance jumpers (JP 6, JP 12, JP 13, JP 14 and TP 1, TP 5) to meet the requirements for impedance and maximum output level.
4. Connect the DVM to the left channel output of the RE 663 ISDN Layer II Decoder and terminate the output with 600 Ω or >25 kΩ, depending on the output impedance of the RE663 ISDN Layer II Decoder.
5. Adjust R117 fully, clockwise.
6. Adjust R30 until the DVM reads the required maximum output level +2.00 dB ±0.05 dB.
7. Adjust R117 until the DVM reads the required maximum output level ±0.05 dB.

### Right Channel Gain Adjustment

1. Connect the RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder to each their ISDN basic rate access, and establish a minimum of four B-channels.
2. Apply the digital audio signal to the RE 662 ISDN Layer II Encoder.
3. Set the gain and output impedance jumpers (JP 10, JP 7 JP 9, JP 8 and TP 6, TP 7) to meet the requirements for impedance and maximum output level.
4. Connect the DVM to the right channel output of the RE 663 ISDN Layer II Decoder and terminate the output with 600 Ω or >25 kΩ, depending on the output impedance of the RE663 ISDN Layer II Decoder.
5. Adjust R116 fully, clockwise.
6. Adjust R96 until the DVM reads the required maximum output level +2.00 dB ±0.05 dB.
7. Adjust R116 until the DVM reads the required maximum output level ±0.05 dB.

## 7.11 Audio Monitor

### 7.11.1 General Description

The audio monitor provides conventional analog headphone monitoring capability of the audio output signals. The monitor is accessible at the front panel along with a volume control.

### 7.11.2 Interfaces

| Signal | Description |
|---|---|
| Left | Left channel analog input signal from the analog audio output circuit |
| Right | Right channel analog input signal from the analog audio output circuit |
| Left | Left channel analog audio output to the front panel headphone jack connector |
| Right | Right channel analog audio output to the front panel headphone jack connector |

*Table 7.12 Input/Output Lines, Analog Audio Output*

### 7.11.3 Circuit Description

Fig. 7.6 shows a block diagram of the audio monitor circuit.

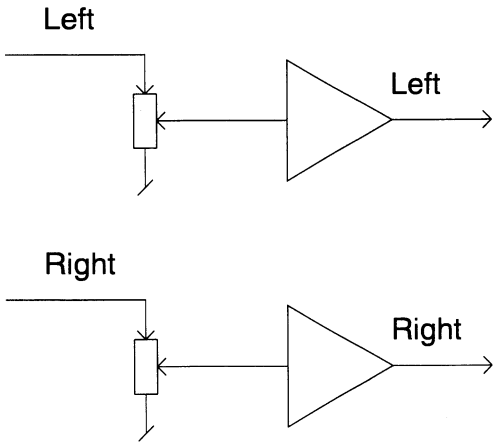


*Fig. 7.6 The Audio Monitor Circuit*

The left and right channel analog input signals are connected to the front panel potentiometer for level adjustment and buffered to drive the stereo headphone output.

## 7.12 Clock Control Circuit

### 7.12.1 General Description

The clock control circuit repeatedly measures the frequency of the clock input from the B-channel equalizer board and forwards the readings to the controller. The controller uses the clock frequency measurement to determine the transmission rate, and hence controls that Layer II frames are decoded accordingly. Secondly, the clock input is used as reference frequency for PLLs restoring the three audio sample frequencies.

### 7.12.2 Interfaces

| Signal | Description |
|---|---|
| CLOCK_A | Layer II bit clock to the Layer II decoder to be associated with DATA_A |
| CLOCK_B | This signal is unused in this configuration |
| DATA_A | Layer II data to the Layer II decoder from the B-channel equalizer board |
| DATA_B | This signal is unused in this configuration |
| 6144 kHz | This signal is unused in this configuration |
| 8192 kHz | Sample frequency output to the analog audio output circuit |
| 11289.6 kHz | Sample frequency output to the analog audio output circuit |
| 12288 kHz | Sample frequency output to the analog audio output circuit |
| AD0;7 | Bi-directional data bus to the controller |
| WR | Write control signal from the controller |
| RD | Read control signal from the controller |
| S8 | Chip enable signal from the controller |
| A0 | Address bit from the controller |
| PUPRES | Power-up reset signal from the controller |
| LCA_DONE | Control signal to the controller confirming that software is downloaded after power-up |
| FRQRDY | Control signal to the controller, clearing for a new clock frequency measure |
| LCA_RDY | Output signal to the controller signaling ready for next data byte during configuration after power-up |
| LCA_INIT | Output signal to the controller signaling ready to start configuration after power-up |

*Table 7.13 Input/Output Lines, Clock Control Circuit*

### 7.12.3 Circuit Description

Fig. 7.7 shows a block diagram of the clock control circuit.

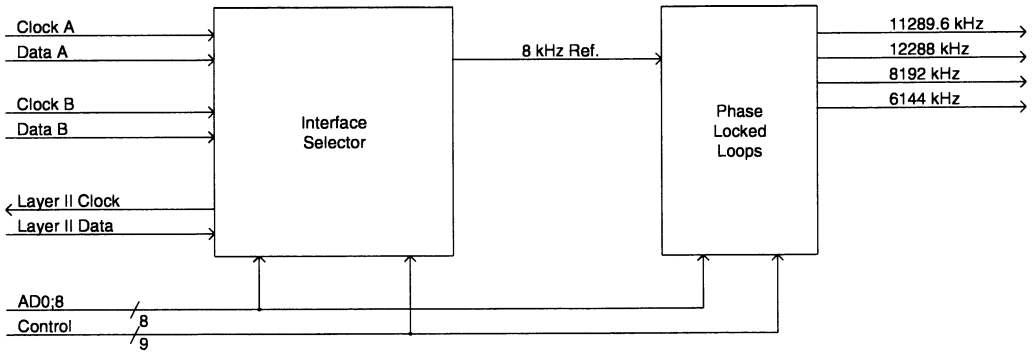


*Fig. 7.7 The Clock Control Circuit*

The clock control circuit is designed in a large logic cell array comprising all the clock selectors, the frequency counter and divider circuitry for the phase locked loops. The block diagram above is intended to give the reader an understanding of the clock control circuit rather than reflecting the actual implementation.

The interface selector circuit, supervised by the controller, sequentially measures the clock input frequency. The input clock signal is divided by M to give an 8 kHz reference signal, to which a 8,192 kHz VCXO is locked. The locked 8,192 kHz clock (the sample frequency output for 32 kHz sampling) is divided by 4 to provide a 2,048 kHz reference signal to lock a 12,288 kHz VCO (the sample frequency output for 48 kHz sampling).

Finally, the 8,192 kHz reference clock is divided by 320 giving a 25.6 kHz reference signal for locking a 11,289.6 kHz VCO (the sample frequency output for 44.1 kHz sampling).

### 7.12.4 Adjustments

Fig. 7.11 shows a diagram of the location of the adjustable components in the decoder. For the clock control circuit the following adjustments can be made:

These adjustments require the use of the following:

- A frequency counter with an accuracy better than 10 ppm at 8192 kHz.
- A DVM or an oscilloscope.

### 8 MHz PLL Adjustment

1. Short-circuit the TP 8.
2. Connect the RE 662 to the RE 663 using a loop-back cable.
3. Connect the DVM or oscilloscope to TP 2.
4. Tune L8 until the frequency counter reads 8,192,000 Hz ±40 Hz.
5. Remove the short-circuit on TP 8.

### 12 MHz PLL Adjustment

1. Short-circuit the TP 8.
2. Connect the RE 662 to the RE 663 using a loop-back cable.
3. Connect the DVM or oscilloscope to TP 4.
4. Tune L15 until the DC voltage in TP 4 is 8 V ±0.5 V.
5. Remove the short-circuit on TP 8.

### 11 MHz PLL Adjustment

1. Short-circuit the TP 8.
2. Connect the RE 662 to the RE 663 using a loop-back cable.
3. Connect the DVM or oscilloscope to TP 3.
4. Tune L13 until the DC voltage in TP 3 is 8 V ±0.5 V.
5. Remove the short-circuit on TP 8.

## 7.13 Digital Audio Output Option

### 7.13.1 General Description

The digital audio output receives the same samples, bit clock and sample identifier signal as the analog audio output. The samples can be sample rate converted, before they are encoded to a serial digital audio bit stream according to the AES/EBU or S/PDIF formats, and routed to the rear panel output connector.

### 7.13.2 Jumper Settings

To cope with either AES/EBU or S/PDIF formats, the jumpers JP3, JP4, and JP3 (on the decoder) should be set as shown in Table 7.14. Fig. 7.11 shows a diagram of the location of the adjustable components in the decoder.

| Digital Audio Output | JP3 | JP4 | JP3 on decoder |
|---|---|---|---|
| AES/EBU[a)] | 1-2 | 1-2 | 1-2 |
| S/PDIF | 2-3 | 2-3 | 2-3 |

*Table 7.14 Digital Audio Outputs*

a. Indicates the default setting from RE TECHNOLOCY AS

### 7.13.3 Interfaces

| Signal | Description |
|---|---|
| | Digital audio output to the rear panel |
| Control | Chip enable and read-write control from the controller |
| ADR | 5-bit parallel address bus from the controller |
| AD | 8-bit parallel bi-directional data bus from the controller |
| WS | Sample identifier from the analog audio output |
| CLK | Bit clock from the analog audio output |
| DATA | Serial data signal comprising both left and right samples from the Layer II decoder |
| INT/EXT | Signal from the controller enabling sample rate conversion |
| INT | Interrupt signal to the controller from the digital audio encoder |
| EBU-SPDIF | Signal to the controller to select AES/EBU or S/PDIF encoding |
| 256XFS | Master clock from the analog audio output |
| MCK | Master clock from the digital reference input |
| E_CLK | Bit clock from the digital reference input |
| E_WS | Word identifier signal from the digital reference input |

*Table 7.15 Input/Output Lines, Digital Audio Output Option*

### 7.13.4 Circuit Description

Fig. 7.8 shows a block diagram of the digital audio output circuit.

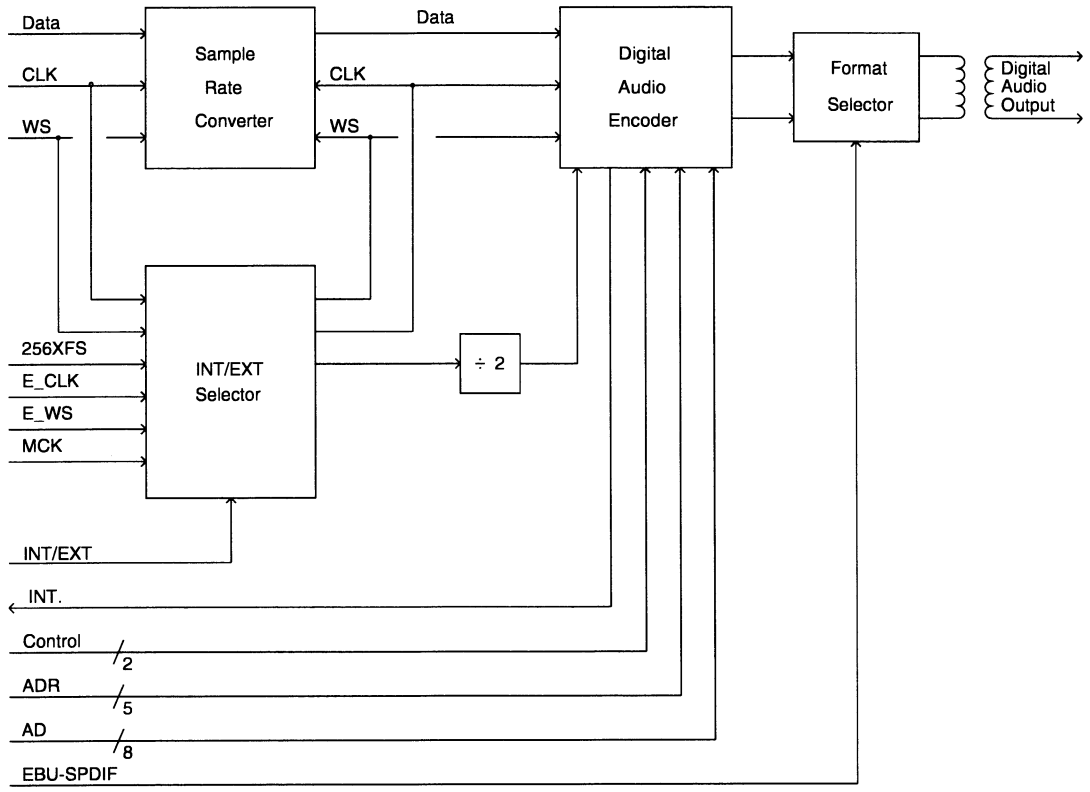


*Fig. 7.8 The Digital Audio Output Circuit*

The audio samples are received from the Layer II Decoder in parallel with the analog audio output. The samples are stored in the sample rate converter using the bit clock and sample identifier signals from the analog audio output circuit.

The sample output rate from the sample rate converter is selected by the controller signal INT/EXT. Position INT is signaled when the digital reference input is not used, and causes the samples from the sample rate converter to be read by the bit clock and sample identifier from the analog audio output circuit. This disables the sample rate conversion, as the output rate equals the input rate.

When a signal is applied to the digital reference input, the controller switches the bit clock and word identifier signal from the digital reference input to read the samples from the sample rate converter (position EXT).

The sample rate converter equalizes the input and output sample rate without any audible impairments to the audio signals in a range from 1:2 to 2:1, which covers conversion from one of the three standard sample frequencies to any other.

The digital audio encoder encodes the audio samples from the sample rate converter to a serial digital data signal, according to the AES/EBU or S/PDIF specifications, with a bit rate of half of the applied master clock (MCL). The encoding of audio signals is supervised by the controller using the control signals and the 8-bit data bus.

The amplitude and impedance of the digital audio output signal is selected, according to one of the two digital audio formats, using internal jumpers in the format selector before being presented at the rear panel output connector.

## 7.14 Digital Reference Input

### 7.14.1 General Description

The digital reference input accepts an input signal according to the AES/EBU or S/PDIF specifications. The sample rate is extracted from the input signal and used for synchronization of the digital audio output signal. The flexibility of the sample rate converter in the digital audio output allows sample rate conversion from any of the three standard sample frequencies to any other.

### 7.14.2 Jumper Settings

To cope with either AES/EBU or S/PDIF formats, the jumpers JP1 and JP2 should be set as shown in Table 7.16. Fig. 7.11 shows a diagram of the location of the adjustable components in the decoder.

| Digital Audio SYNC Input | JP1 | JP2 |
|---|---|---|
| AES/EBU[a)] | 1-2 | 1-2 |
| S/PDIF | 2-3 | 2-3 |

*Table 7.16 Digital Audio SYNC Inputs*

a. Indicates the default setting from RE TECHNOLOGY AS.

### 7.14.3 Interfaces

| Signal | Description |
|---|---|
| | Digital reference input from the rear panel connector |
| 12288 kHz | Reference frequency from the clock control circuit |
| INT | Interrupt signal to the controller signaling a change in the digital reference input |
| Control | Two signals that allow the controller to control the input |
| ADR | 4-bit address bus from the controller |
| AD | 8-bit bi-directional data bus from the controller |
| E_WS | Sample identifier signal (sample frequency) to the digital audio output circuit |
| E_CLK | Bit clock, corresponding to E_WS, to the digital audio output circuit |
| MCK | Master clock to the digital audio output circuit, derived from the input signal |

*Table 7.17 Input/Output Lines, Digital Reference Input*

### 7.14.4 Circuit Description

Fig. 7.9 shows a block diagram of the digital reference input circuit.

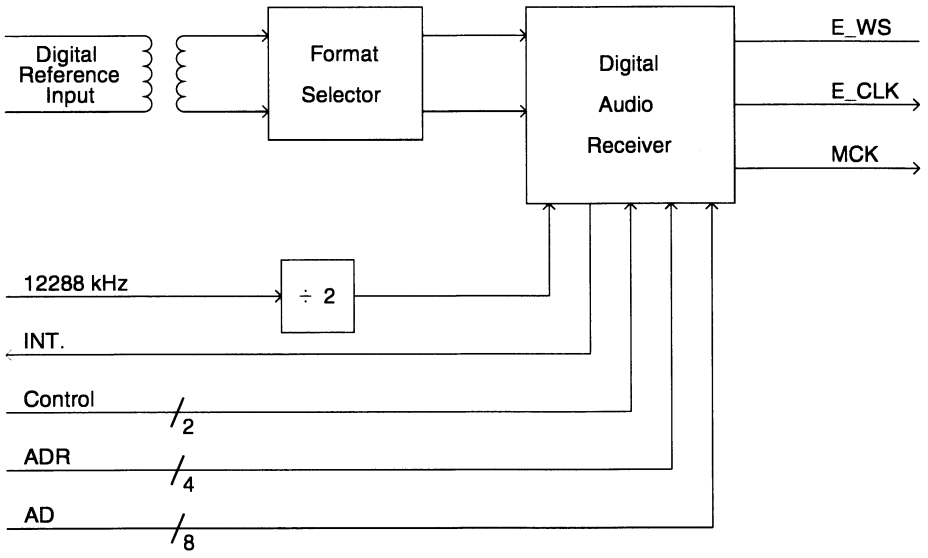


*Fig. 7.9 The Digital Reference Input Circuit*

The digital reference input signal is a digital audio signal according to the AES/EBU or S/PDIF specifications. The format selector contains an internal jumper setting allowing conformance to either of the two input formats.

A transformer provides a galvanic separation of the input from the reference source before the input signal enters the digital audio receiver circuit. This circuit is supervised by the controller, and extracts the sample frequency and bit clock timing, which is fed to the digital audio output circuit, for synchronization and sample rate conversion of the digital audio output.

When a digital reference signal is applied, the controller lights the green "DIG. LOCK" LED on the front panel of the RE 663 ISDN Layer II Decoder, and the digital audio output signal is automatically synchronized to the applied reference. The sample frequency used within the Layer II transmission from the RE 662 ISDN Layer II Encoder to the RE 663 ISDN Layer II Decoder is shown in both the encoder and decoder displays. Despite this sample frequency, the sample frequency used in the digital audio output from the RE 663 ISDN Layer II Decoder contains the sample frequency from the digital reference input, whenever the green front panel LED is on.

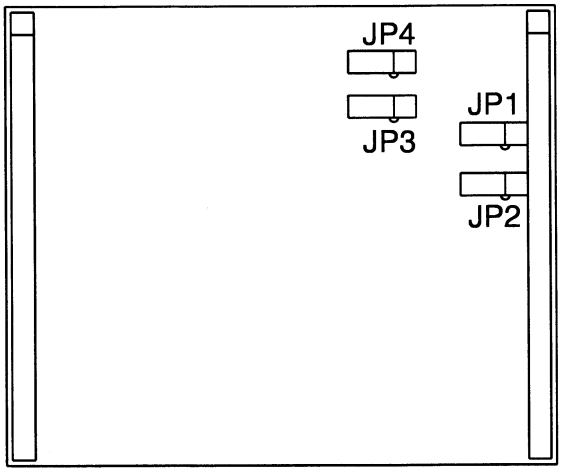


*Fig. 7.10 Adjustable Components, Digital Reference Input*

## 7.15 Adjustable Components

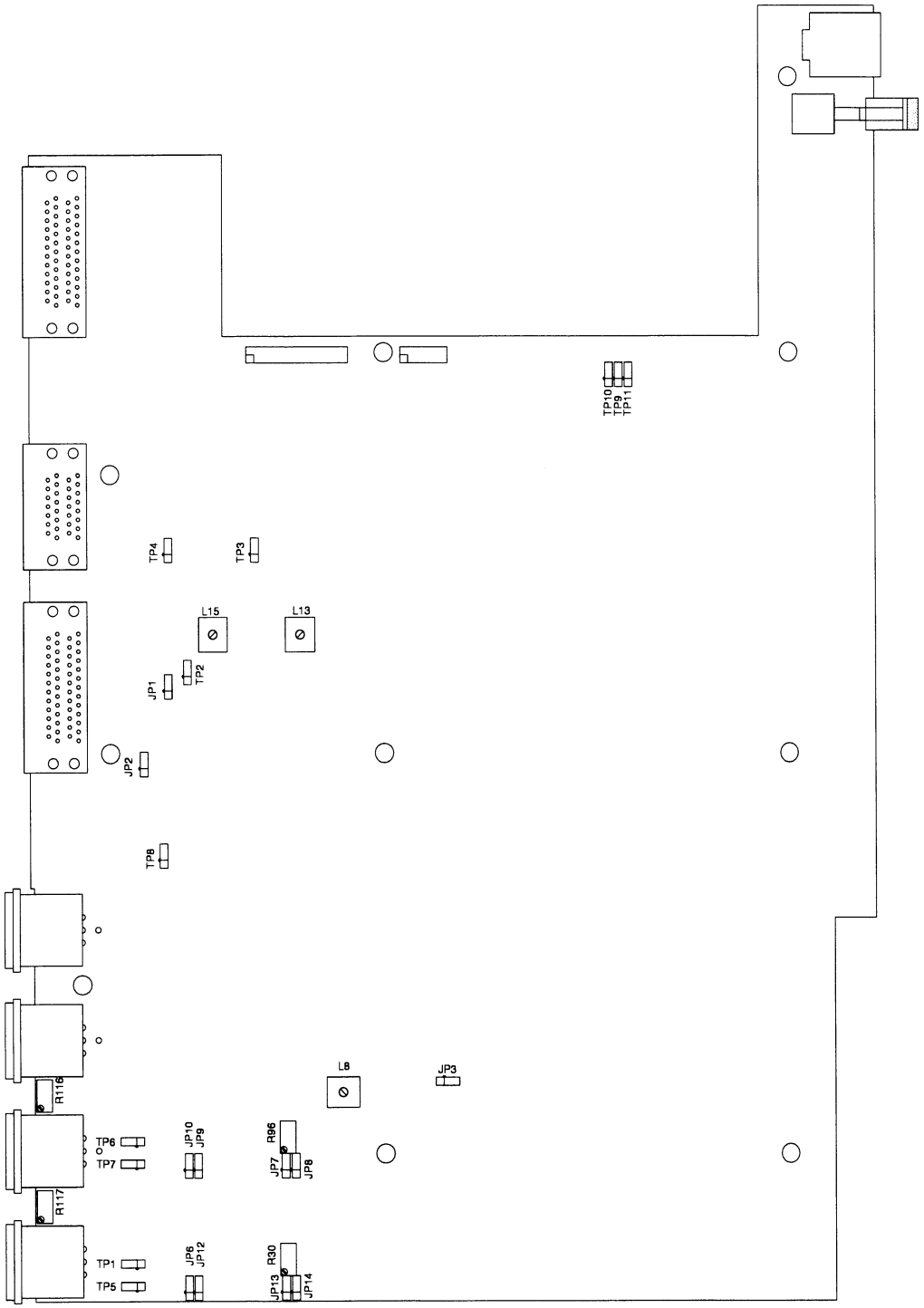


*Fig. 7.11 Adjustable Components in the Decoder Circuits*

# 8. Power Supply

## 8.1 AC Power Supply

The RE 662 ISDN Layer II Encoder and the RE 663 ISDN Layer II Decoder must be powered from an AC source.

The power supply is a commercially available, miniature, 40 W, switch-mode, AC supply. It must be used together with an AC mains power source.

It is capable of supplying regulated +5 V, +15 V and -15 V DC from a line voltage of 90 to 250 V AC with a frequency range of 47 to 65 Hz. Furthermore, MOSFET-based switching circuits allow for output regulation down to zero load. Table 8.1 shows the DC output connector (J2) from the power supply.

| J2 Pin | Signal |
|---|---|
| 1 | +15 V regulated |
| 2 | +5 V regulated |
| 3 | +5 V regulated |
| 4 | Ground |
| 5 | Ground |
| 6 | -15 V regulated |

*Table 8.1 Power Supply Output Connector (J2) Pin-out*

# 9. Equipment and Accessories

This chapter contains a list of the accessories supplied with the RE 662 and RE 663 ISDN Layer II Codec and a list of optional equipment and accessories.

## 9.1 Standard Equipment and Accessories

The following equipment and accessories should be found when unpacking the RE 662 ISDN Layer II Encoder or the RE 663 ISDN Layer II Decoder.

| Order number | Description |
|---|---|
| 395-028 | RE 662 ISDN Layer II Encoder, **or** |
| 395-029 | RE 663 ISDN Layer II Decoder |
| 983-483 | Operator Manual |

*Table 9.1 Standard Equipment and Accessories*

## 9.2 Optional Equipment and Accessories

Optional equipment and accessories to be used with the RE 662 and RE 663 ISDN Layer II Codec.

| Order number | Description |
|---|---|
| 910-314 | Handset |
| 906-797 | 384 kbit/s Option |
| 902-416 | Digital Audio Input Option |
| 902-417 | Digital Audio Output Option |
| 618-276 | $S_0$ Cable |
| 983-486 | Service Manual |

*Table 9.2 Optional Equipment and Accessories*

# 10. Specifications

This chapter contains the full specifications for the encoder and the decoder. The listed data is guaranteed.

## Analog Audio Specifications

| | |
|---|---|
| Type of connector | 3-pin XLR, female for inputs and male for outputs |
| Companding | ISO/MPEG Layer II or G.722 |
| A/D and D/A converter resolution | 16 bits sigma-delta, 64/128 times over-sampling |
| Sampling frequency | Selectable: 16, 22.05, 24, 32, 44.1 or 48 kHz |
| Input impedance | 600 Ω or >25 kΩ, balanced |
| Nominal input level | +6, +3, 0, -3, -6, -9, -12, -15 or -18 dBr |
| Clipping level | +15dBm0 |
| Output impedance | 600 Ω or <60 Ω, balanced |
| Nominal output level | |
| (<60 W) | +9, +6, +3, 0, -3, -6, -14, -17 or -20 dBr |
| (600 W) | +3, 0, -3, -6, -9, -12, -20, -23 or -26 dBr |
| Maximum output level | +015 dBm0 |
| Insertion gain | 0 dB ±0.2 dB |

## Layer II Coding[1)]

| | |
|---|---|
| Frequency response[2)] | ±0.30 dB relative to 1 kHz |
| Fs = 16 kHz | 20 to 7,500 Hz |
| Fs = 22.05 kHz | 20 to 10,300 Hz |
| Fs = 24 kHz | 20 to 11,250 Hz |

1) The analog audio specifications are given for a codec pair coupled back-to-back at 384 kbit/s stereo transmission rate, unless otherwise stated.
2) This specification covers a codec pair coupled back-to-back at 128 kbit/s stereo transmission rate.

| | |
|---|---|
| Frequency response | ±0.15 dB relative to 1 kHz |
| Fs = 32 kHz | 20 to 14,500 Hz |
| Fs = 44.1 kHz | 20 to 20,000 Hz |
| Fs = 48 kHz | 20 to 20,000 Hz |
| Total harmonic distortion | |
| 3 dB below clipping, 1kHz | <-80 dB at 1 kHz |
| SINAD | |
| 3 dB below clipping, 1kHz | <-60 dB at 1 kHz |
| Idle channel noise, +15 dBm0 clipping | |
| Quasipeak, unweighted | <-67 dBq0 |
| Quasipeak, weighted | <-60 dBq0ps |
| RMS, unweighted | <-71 dBm0 |
| Signal-to-Noise ratio | >86 dB |
| Crosstalk | <-85 dB |
| Phase difference between channels | <3× |
| Delay | |
| Fs = 16 kHz | <310 ms |
| Fs = 22.05 kHz | <225 ms |
| Fs = 24 kHz | <210 ms |
| Fs = 32 kHz | <160 ms |
| Fs = 44.1 kHz | <120 ms |
| Fs = 48 kHz | <110 ms |

| Maximum Bandwidth vs. Bit Rates and Audio Modes | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit Rate (kbit/s)** | **Audio Mode** | | | | **Bandwidth (kHz) vs. Sampling Frequency** | | | | | | |
| | **Mono** | **Dual** | **Stereo** | **Joint Stereo** | | **16 kHz** | **22.05 kHz** | **24 kHz** | **32 kHz** | **44.1 kHz** | **48 kHz** |
| 56 | ✓ | | | | 1 ch. | 7.5 | 10.3 | 11.2 | 6.8 | 9.4 | 10.2 |
| 64 | ✓ | ✓ | ✓ | ✓ | 1 ch. | 7.5 | 10.3 | 11.2 | 6.8 | 9.4 | 10.2 |
| | | | | | 2 ch. | 7.5 | 10.3 | 11.2 | 6.0 | 5.5 | 6.0 |
| 112[a)] | ✓ | ✓ | ✓ | ✓ | 1 ch. | 7.5 | 10.3 | 11.2 | 15.0 | 20.6 | 20.2 |
| | | | | | 2 ch. | 7.5 | 10.3 | 11.2 | 6.8 | 9.4 | 10.2 |
| 128[a)] | ✓ | ✓ | ✓ | ✓ | 1 ch. | 7.5 | 10.3 | 11.2 | 15.0 | 20.6 | 20.2 |
| | | | | | 2 ch. | 7.5 | 10.3 | 11.2 | 6.8 | 9.4 | 10.2 |
| 192 | ✓ | ✓ | ✓ | ✓ | 1 ch. | - | - | - | 15.0 | 20.6 | 20.2 |
| | | | | | 2 ch. | - | - | - | 15.0 | 20.6 | 20.2 |
| 256 | - | ✓ | ✓ | ✓ | 2 ch. | - | - | - | 15.0 | 20.6 | 20.2 |
| 320 | - | ✓ | ✓ | ✓ | 2 ch. | - | - | - | 15.0 | 20.6 | 20.2 |
| 384 | - | ✓ | ✓ | ✓ | 2 ch. | - | - | - | 15.0 | 20.6 | 20.2 |

*Table 10.1 Maximum Bandwidth vs. Bit Rates and Audio Modes*

a. In the joint stereo mode the bandwidth is : 32 kHz sampling rate - 13.5 kHz. 44.1 kHz sampling rate - 18.6 kHz. 48 kHz sampling rate - 20.2 kHz.

## G.722 Coding

Frequency response

| | |
|---|---|
| Relative to 1 kHz | ±0.3 dB, 20 to 6400 Hz |
| | +0.3/-3.0 dB, 20 to 7000 Hz |

Total harmonic distortion

| | |
|---|---|
| 3 dB below clipping, 1kHz | <-50 dB |

SINAD

| | |
|---|---|
| 3 dB below clipping, 1kHz | <-46 dB, 64 kbit/s Mode 1 |
| | <-40 dB, 64 kbit/s Mode 2 |
| | 56 kbit/s |

| | |
|---|---|
| Idle channel noise, +15 dBm0 clipping | |
| Quasipeak, unweighted | <-55 dBq0 |
| Quasipeak, weighted | <-44 dBq0ps |
| RMS, unweighted | <-60 dBm0 |
| Signal-to-Noise ratio | >75 dB |
| Group Delay Variation | <0.05 ms |

## Auxiliary Data Channel Specifications

| | |
|---|---|
| Type of connector | 25-pin Sub-D, female |
| Baud rate | |
| LayerII | 300, 600, 1200, 2400, 4800 or 9600 baud |
| G.722 | 9600 baud |
| Mode | 8 data bits, no parity bit, and 1 stop bit (8N1) |
| Data flow control | Hardware handshake |

## Data Interface Specifications

| | |
|---|---|
| Network Interface | |
| Type | ISDN S0 (2B+D) |
| With 384 kbit/s option | |
| Number of channels | From 1 to 3 in parallel (up to 6 B-channels) |
| Bit rates | 56, 64, 112, 128, 192, 256, 320, or 384 kbit/s |
| Without 384 kbit/s option | |
| Number of channels | 1 (2 B-channels) for audio calls, and 1 B-channel for voice calls |
| Bit rates | 56, 64, 112 or 128 kbit/s |
| ISDN Protocols | |
| | Euro ISDN |
| | 1TR6 |
| | US-NI1 |
| | Australian |

| | |
|---|---|
| X.21/RE660/661 Interface | |
| Type of connector | 15-pin, Sub-D, female |
| Number of channels | Up to 2 |
| Clock/Data signals | V.11/RS-422-A with pin-out according to X.21 |
| Alarm Remote Interface | |
| Type of connector | 25-pin, Sub-D, female |
| Functions | RE 662: Remote control, alarms,<br>RE 663: Remote group call, monitoring, alarms |

## Digital Audio Specifications

| | |
|---|---|
| Type of connector | 3-pin XLR, female for inputs and male for outputs |
| Data format | AES/EBU or S/PDIF |
| Impedance | 110 Ω, balanced or 75 Ω, single ended |
| Lock range | ±400 ppm |

## General Specifications

### Environmental Conditions

| | |
|---|---|
| Storage temperature | -40 to 70 °C (-40 to 158 °F) |
| Operating temperature | 5 to 45 °C (41 to 113 °F) |
| Relative humidity | 20 to 80 %, non-condensing |
| EMC | [3] EN 55022:1986,<br>EN 50082-1:1992 |

### Power Supply

| | |
|---|---|
| Input voltage | 90 to 250 V AC |
| Frequency | 47 to 65 Hz |

3) Shielded cables must be used

| | |
|---|---|
| Power consumption | Approx. 30 VA per terminal |
| Type of connector | IEC standard, single-fused with filter |
| Fuse | Slow Blow, 500 mA |

## Dimensions and Weight

| | |
|---|---|
| Height | 2 U equal to 89 mm (3.5") |
| Width | 482 mm (19") |
| Depth | 310 mm (12.2") |
| Net weight | Approx. 4.5 kg (10 lbs) |
| Shipping weight | Approx. 8.9 kg (19.6 lbs) |

Data subject to change.

# 11. Glossary

The following is a list of the abbreviations used in this Service Manual:

| | |
|---|---|
| AC | Alternating Current |
| ADC | Analog to Digital Conversion |
| AES | Audio Engineering Society |
| AN/DIG | Analog-Digital |
| BSW | Bank SWitch signal |
| CONRDY | CONtroller ReaDY |
| CPU | Central Processing Unit |
| CTS | Clear To Send |
| DAC | Digital to Analog Conversion |
| DC | Direct Current |
| DCD | Data Carrier Detect |
| DCE | Data Communication Equipment |
| DEX | Data EXchange port |
| DFCON | Data From CONtroller |
| DFDSP | Data From Digital Signal Processor |
| DIL | Dual In Line |
| DMD | Data Memory Data bus |
| DSC | Digital Subscriber Controller , |
| DSP | Digital Signal Processor |
| DSPRDY | Digital Signal Processor ReaDY |
| DSR | Data Set Ready |
| DVM | Digital VoltMeter |
| E | Enable |
| EBU | European Broadcasting Union |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| EPROM | Erasable and Programmable Read Only Memory |
| FET | Field Effect Transmitter |
| FIFO | First In First Out |

| | |
|---|---|
| FSC | Franm Sync signal |
| HDLC | High Data Link Channel |
| ICR | Inter City Relays |
| IEC | International Electrotechnical Commission |
| ISDN | Integrated Services Digital Network |
| ISO | The International Organization for Standardization |
| ITAC | ISDN Terminal Adapter Circuit |
| ITU-R | International Telecommunications Union-Radiocommunication Sector |
| ITU-T | International Telecommunications Union-Telecommunication Sector |
| LCA | Logic Cell Array |
| LED | Light Emitting Diode |
| LSB | Least Significant Bit |
| MCL | Master CLock |
| MOSFET | Metal Oxide Semiconductor Field Effect Transmitter |
| MPEG | Moving Pictures Experts Group |
| MSB | Most Significant Bit |
| NA | Not Applicable |
| NT | Network Termination |
| PAL | Phase Alternating Line |
| PCB | Printed Circuit Board |
| PLL | Phase Locked Loop |
| PROM | Programmable Read Only Memory |
| R/W | Read/Write |
| RAM | Random Access Memory |
| RS | Register Select |
| RTS | Request To Send |
| S/PDIF | Sony/Philips Digital InterFace |
| SP | Solder Point |
| STL | Studio-to-Transmitter Links |
| TBRI | Triple Base Rate Interface |
| TE | Terminal Equipment |
| TP | Test Point |

| | |
|---|---|
| TTL | Transistor-Transistor Logic |
| UART | Universal Asynchronous Receiver Transmitter |
| VCO | Voltage-Controlled Oscillator |
| VCXO | Voltage-Controlled Crystal Oscillator |

# 12. Index

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| | |
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